AS05N06M-Q1

N-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
60V	43mΩ@10V	5A
	47mΩ@4.5V	

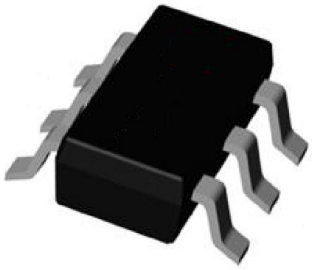
Feature

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- Suffix "-Q1" for AEC-Q101

Application

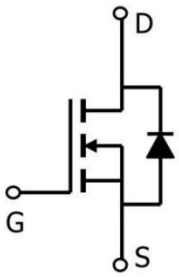
- PWM application
- Load switch

Package

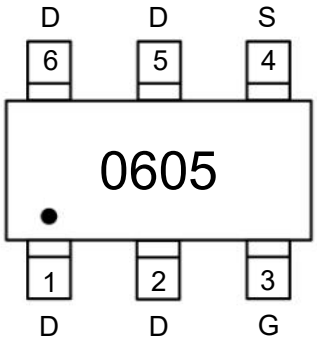


SOT-23-6L

Circuit diagram



Marking



AS05N06M-Q1

N-Channel Enhancement Mode MOSFET

Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	5	A
Continuous Drain Current(T_A=70℃)	I_D(70℃)	4	
Pulsed Drain Current[1)]	I_{DM}	20	A
Power Dissipation	P_D	1.25	W
Thermal Resistance from Junction to Ambient[2)]	$R_{\theta JA}$	100	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_J=25 ºC, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =60V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.0	1.5	2.5	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D =5A		34	43	mΩ
		V_{GS} =4.5V, I_D =4A		36	47	
Dynamic characteristics[3)]						
Input Capacitance	C_{iss}	V_{DS} =30V,V_{GS} =0V,f =1MHz		1018		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			62		
Total Gate Charge	Q_g	V_{DS} =30V,V_{GS} =10V, I_D =5A		26.4		nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			6.5		
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V,V_{GS}=10V,I_D=2A R_{GEN}=3Ω,R_L=1Ω		10		nS
Turn-on rise time	t_r			20		
Turn-off delay time	$t_{d(off)}$			29		
Turn-off fall time	t_f			21		
Source-Drain Diode characteristics						
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S=5A			1.2	V
Reverse Recovery Charge	Q_{rr}	I_F=5A,di/dt=500A/μs		11.7		nC
Reverse Recovery Time	t_{rr}			23		nS

Notes:

1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

2) $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

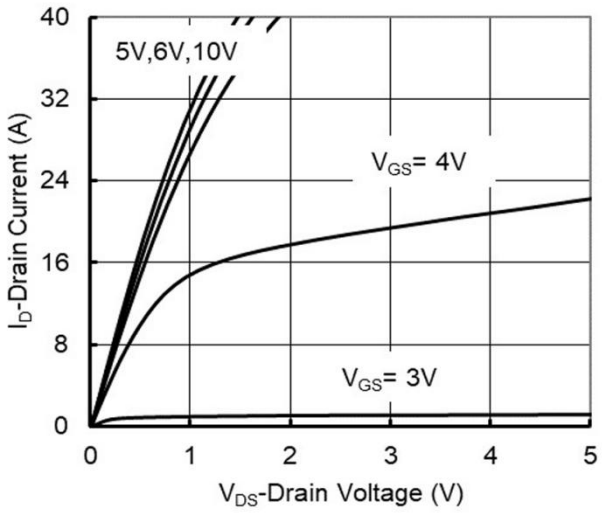


Figure 1. Output Characteristics

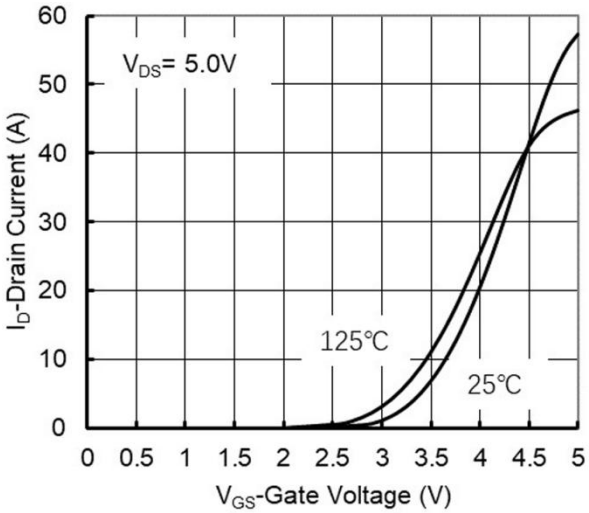


Figure 2. Transfer Characteristics

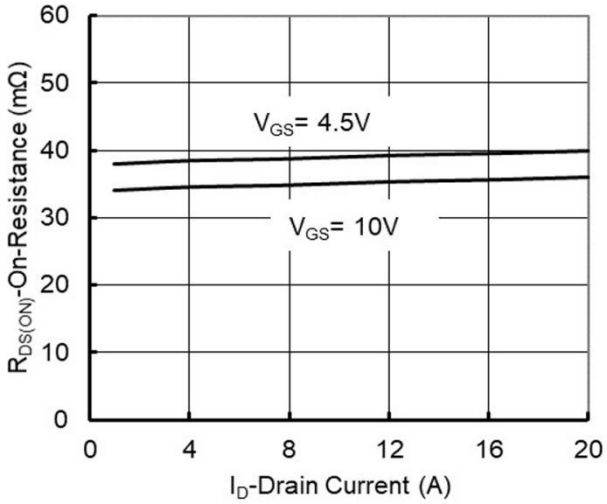


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

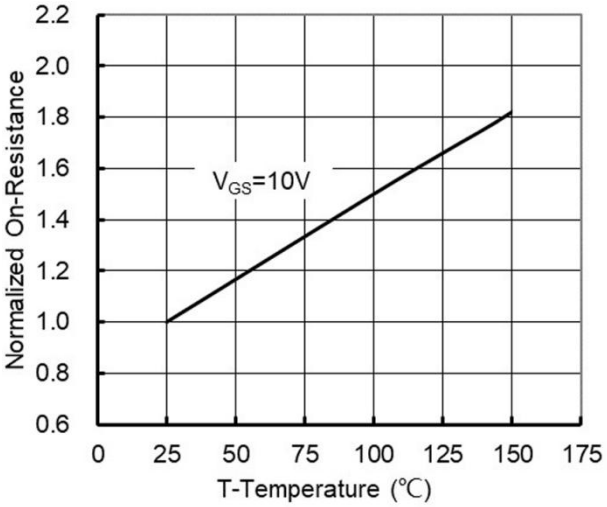


Figure 4. On-Resistance vs. Junction Temperature

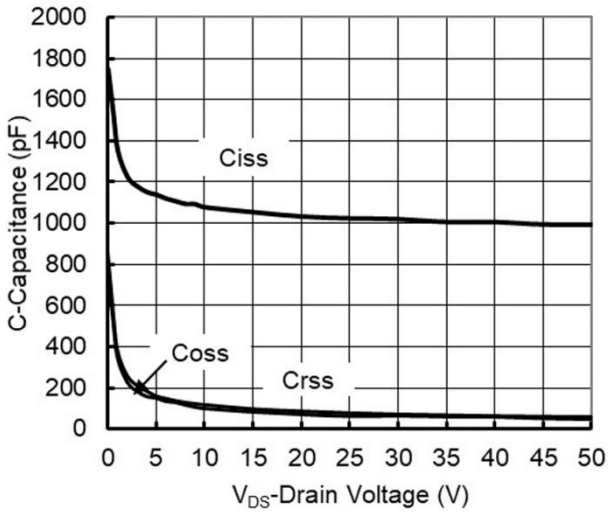


Figure 5. Capacitance Characteristics

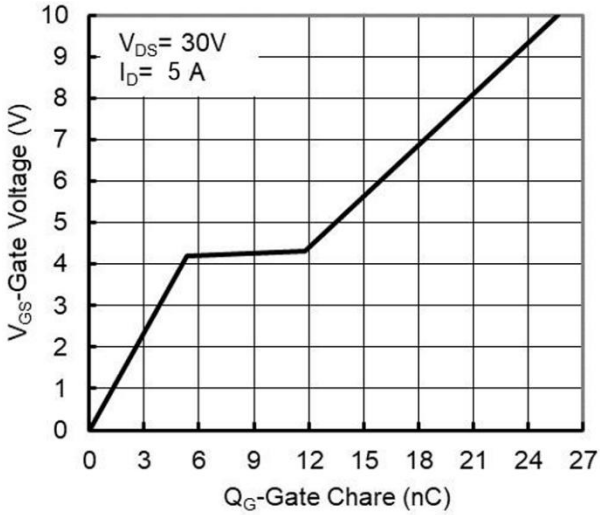


Figure 6. Gate Charge

Typical Characteristics

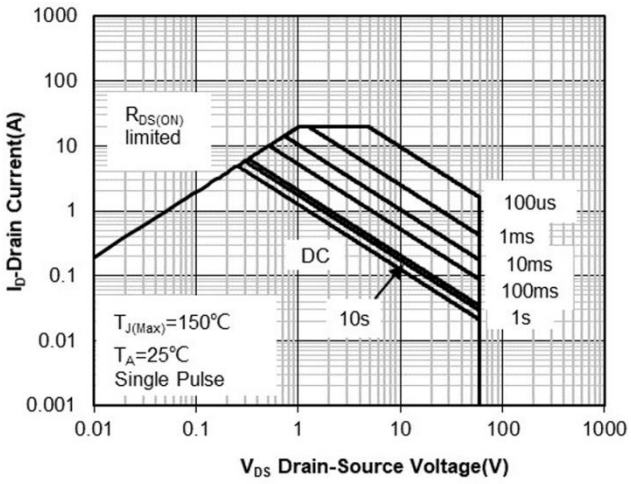


Figure 7. Safe Operation Area

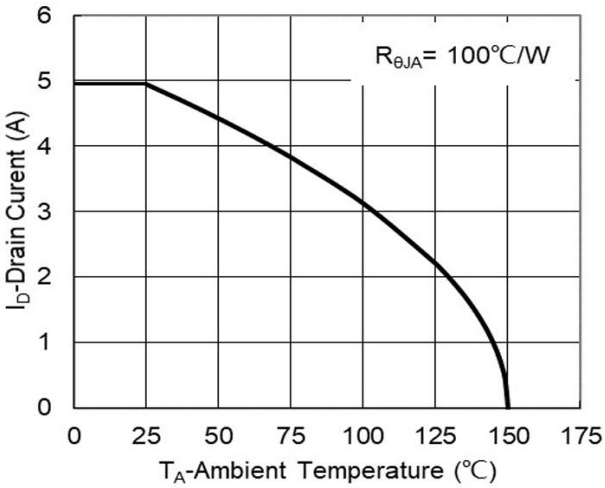


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

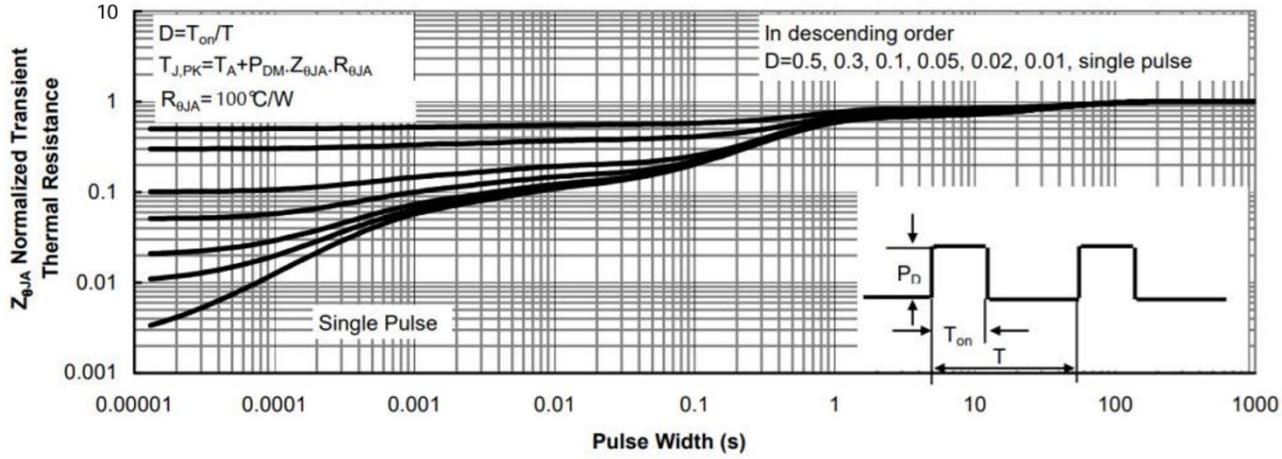
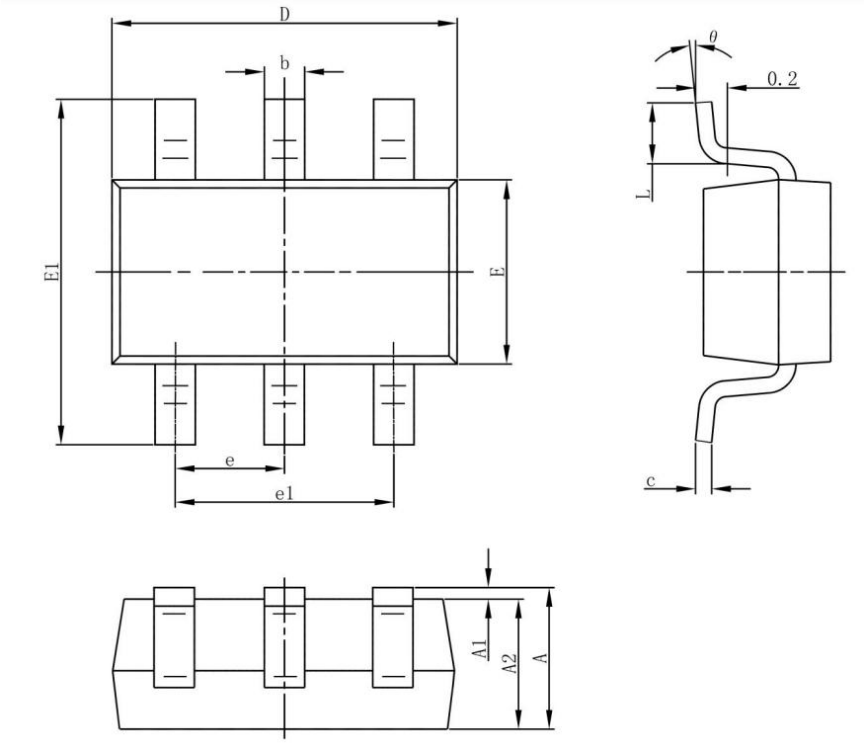


Figure 9. Normalized Maximum Transient Thermal Impedance

SOT-23-6L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°