# AS05N10FL

N-Channel Enhancement Mode MOSFET

## Product Summary

| $V_{(BR)DSS}$ | $R_{DS(on)MAX}$ | $I_D$ |
|---|---|---|
| 100V | 36mΩ@10V | 4.7A |
| | 48mΩ@4.5V | |

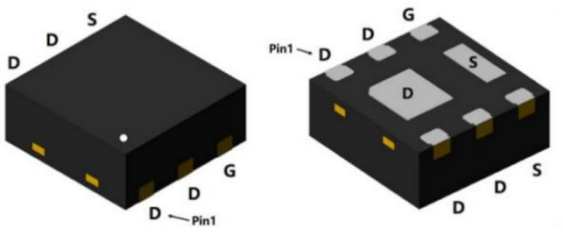
## Feature

- Low gate charge
- Low input capacitance
- Lead-free parts meet RoHS requirements

## Application

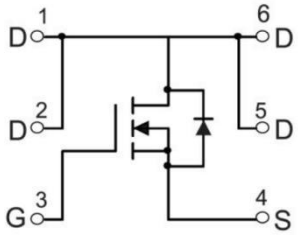
- PWM application
- Load switch
- Battery charge in cellular handset

## Package

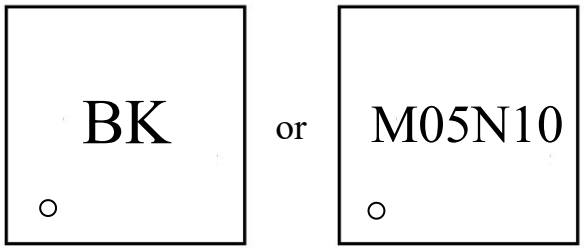



DFN2*2-6L

## Circuit diagram




## Marking



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N-Channel Enhancement Mode MOSFET

## Absolute maximum ratings ($T_C$=25℃ unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[1] ($T_A$=25℃) | $I_D$ | 4.7 | A |
| Continuous Drain Current[1] ($T_A$=70℃) | $I_D$(70℃) | 3.8 | A |
| Pulsed Drain Current[2] | $I_{DM}$ | 18.8 | A |
| Avalanche current[2] | $I_{AS}$ | 16 | A |
| Avalanche energy[3] | $E_{AS}$ | 12.8 | mJ |
| Power Dissipation[4]($T_A$=25℃) | $P_D$ | 1.5 | W |
| Thermal Resistance,Junction-to-Ambient | $R_{\theta JA}$ | 85 | ℃/W |
| Junction Temperature | $T_J$ | 150 | ℃ |
| Storage Temperature | $T_{STG}$ | -55 ~ +150 | ℃ |

## Electrical characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$= 0V, $I_D$ =250μA | 100 | | | V |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ =80V,$V_{GS}$ = 0V | | | 1 | μA |
| Gate-body leakage current | $I_{GSS}$ | $V_{GS}$ =±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ =250μA | 1.2 | 1.9 | 2.5 | V |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_{GS}$ =10V, $I_D$ =4.5A | | 29 | 36 | mΩ |
| | | $V_{GS}$ =4.5V, $I_D$ =4A | | 37 | 48 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ =5V, $I_D$ =4.5A | | 14 | | S |
| **Dynamic characteristics[5]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ =50V,$V_{GS}$ =0V,f =1MHz | | 363 | | pF |
| Output Capacitance | $C_{oss}$ | | | 85 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 3 | | |
| Gate Resistance | $R_g$ | f = 1.0MHz | | 1.7 | | Ω |
| Total Gate Charge | $Q_g$ | $V_{DS}$ =50V,$V_{GS}$ =10V, $I_D$ =4.5A | | 6.8 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 1.8 | | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DS}$=50V,$V_{GS}$=10V, $R_L$=11Ω,$R_{GEN}$=6Ω | | 4.9 | | nS |
| Turn-on rise time | $t_r$ | | | 16.6 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 11.2 | | |
| Turn-off fall time | $t_f$ | | | 4.9 | | |
| **Source-Drain Diode characteristics** | | | | | | |
| Diode forward current | $I_S$ | $T_C$=25℃ | | | 1 | A |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$ =0V, $I_S$=1A | | | 1.2 | V |
| Reverse recovery time | $t_{rr}$ | $I_F$ =4.5A, $dI_F/dt$=100A/us | | 33 | | nS |
| Reverse recovery charge | $Q_{rr}$ | | | 45 | | nC |

Notes:

1) Computed continuous current assumes the condition of $T_{J\text{-}MAX}$ while the actual continuous current depends on the thermal J_MAX & electro-mechanical application board design.

2) This single-pulse measurement was taken under $T_{J\text{-}MAX}$ =150℃

3) This single-pulse measurement was taken under the following condition [ L =100uH, $V_{GS}$ =50V] while its value is limited by $T_{J\text{-}MAX}$ =150℃

4) The power dissipation $P_D$ is based on $T_{J\text{-}MAX}$ =150℃

5) Guaranteed by design, not subject to production.

## Typical Characteristics

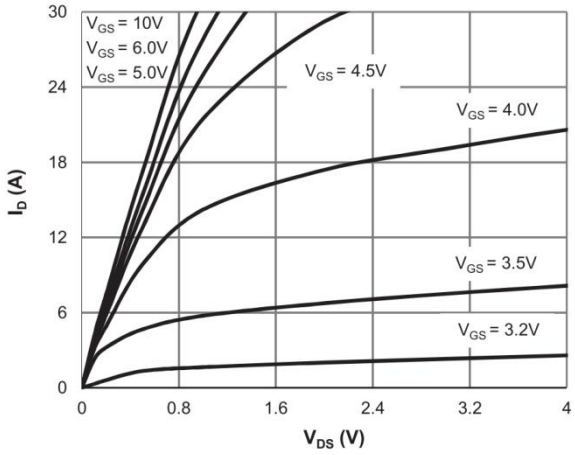



Figure 1: Saturation Characteristics

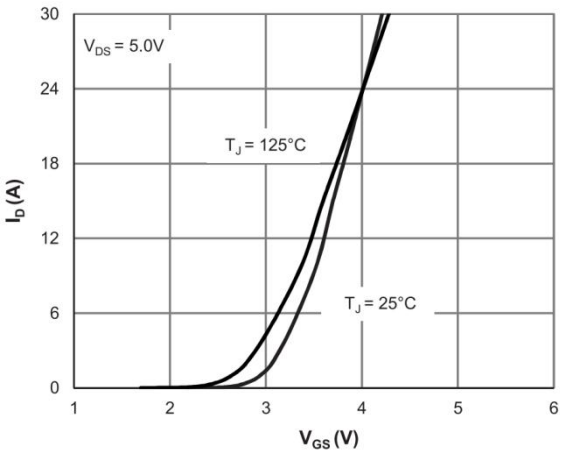



Figure 2: Transfer Characteristics

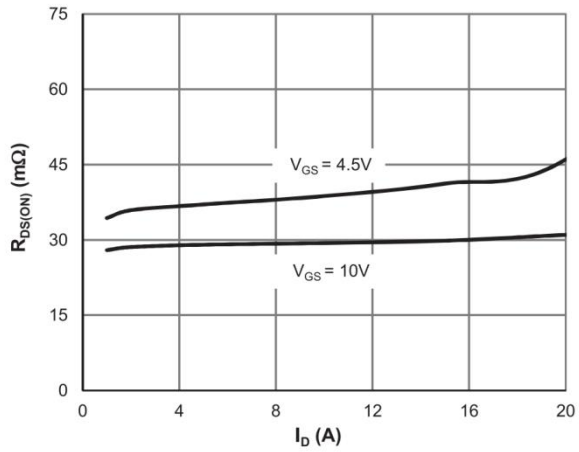



Figure 3: $R_{DS(ON)}$ vs. Drain Current

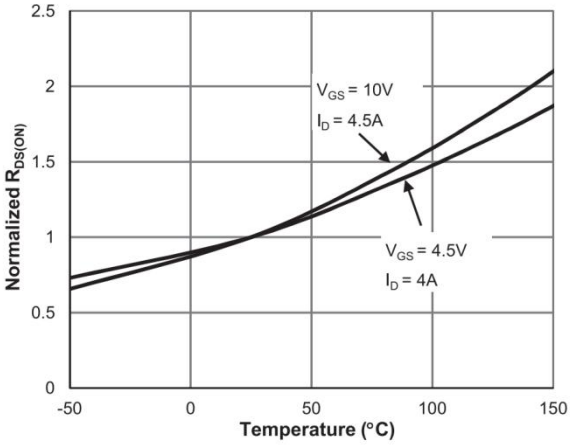



Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

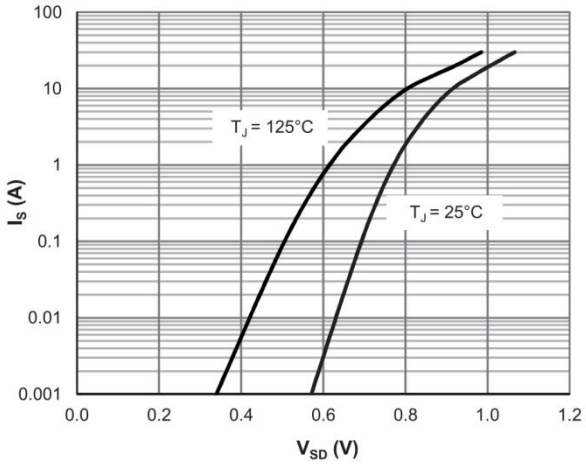



Figure 5: Body-Diode Characteristics

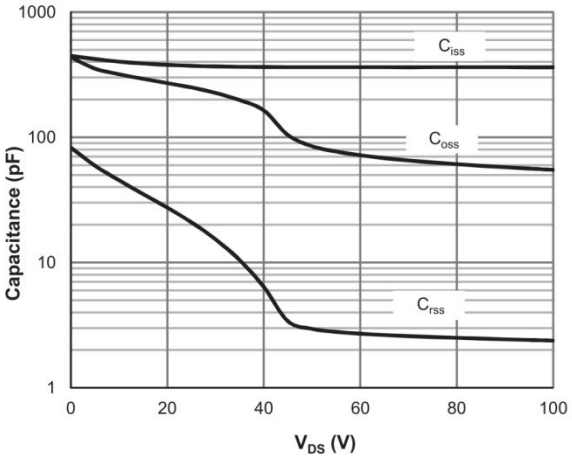



Figure 6: Capacitance Characteristics

## Typical Characteristics

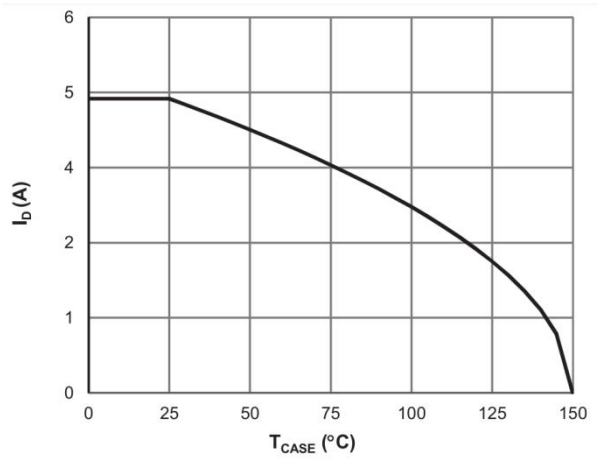



Figure 7: Current De-rating

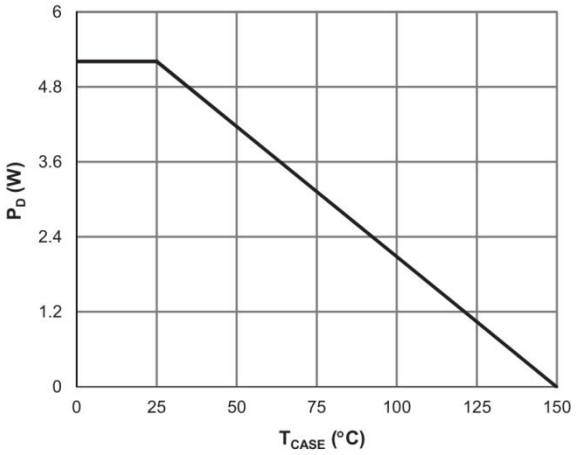



Figure 8: Power De-rating

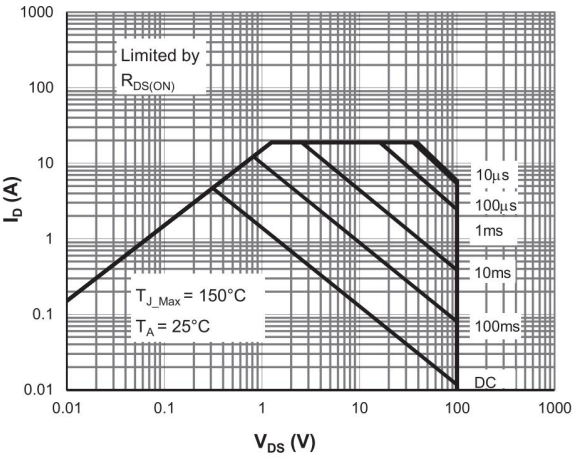



Figure 9: Maximum Safe Operating Area

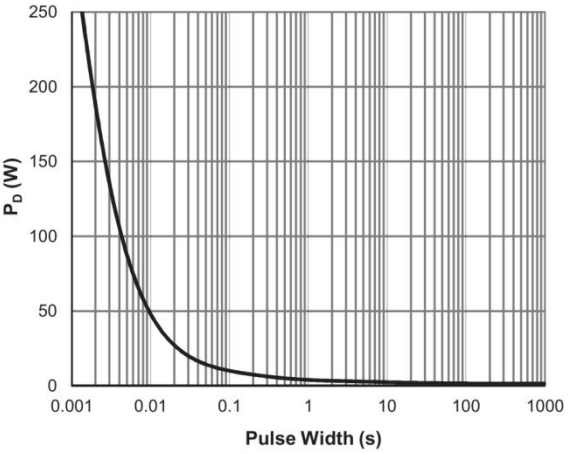



Figure 10: Single Pulse Power Rating, Junction-to-Case

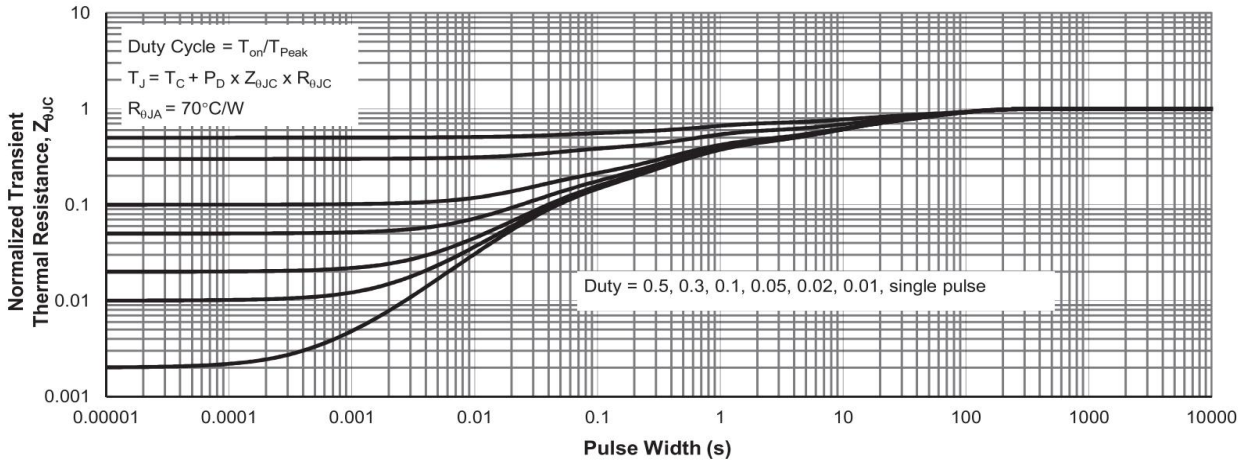



Figure 11: Normalized Maximum Transient Thermal Impedance

## Typical Characteristics

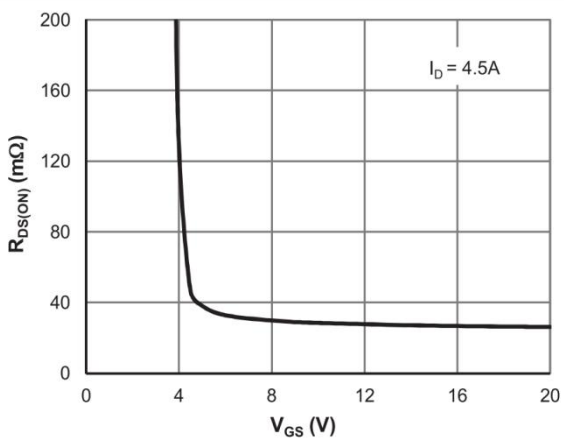



**Figure 12 : $R_{DS(ON)}$ vs. $V_{GS}$**

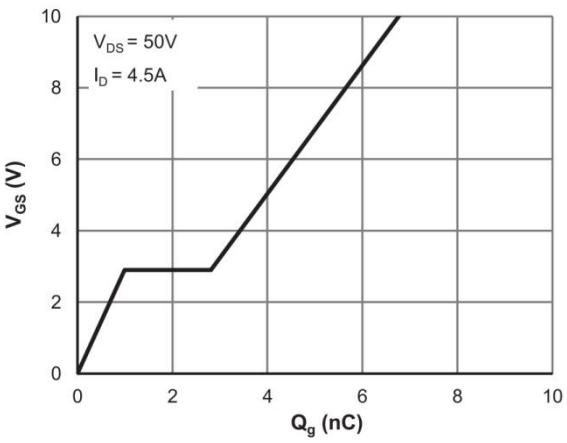
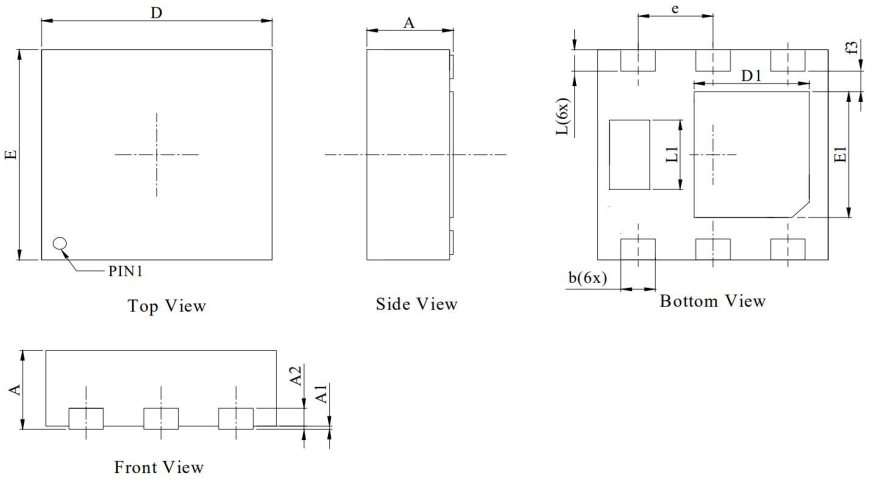



**Figure 13 : Gate Charge**

## DFN2*2-6L Package Information




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | - | 0.050 | - | 0.002 |
| A2 | - | 0.250 | - | 0.010 |
| D | 1.900 | 2.100 | 0.075 | 0.083 |
| E | 1.900 | 2.100 | 0.075 | 0.083 |
| D1 | 0.900 | 1.100 | 0.035 | 0.043 |
| E1 | 1.100 | 1.300 | 0.043 | 0.051 |
| b | 0.250 | 0.350 | 0.010 | 0.014 |
| L | 0.150 | 0.250 | 0.006 | 0.010 |
| L1 | 0.610 | 0.71 | 0.024 | 0.028 |
| e | 0.650 BSC. | | 0.026 BSC. | |
| f3 | 0.150 REF. | | 0.006 REF. | |