AS06P04FL-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-40V	33mΩ@-10V	-6A
	45mΩ@-4.5V	

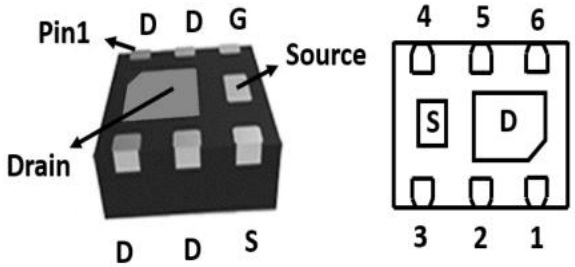
Feature

- Advanced trench MOSFET process technology
- Ultra low on-resistance with low gate charge
- Suffix "-Q1" for AEC-Q101

Application

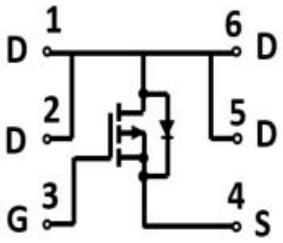
- PWM applications
- Load switch
- Battery charge in cellular handset

Package

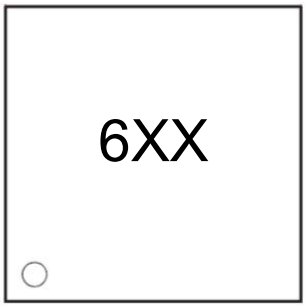


DFN2*2-6L

Circuit diagram



Marking



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P-Channel Enhancement Mode MOSFET

Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	-6	A
Pulsed Drain Current[1]	I_{DM}	-38	A
Power Dissipation	P_D	2.1	W
Thermal Resistance Junction-to-Ambient[2]	$R_{\theta JA}$	59.5	℃/ W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-40			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-40V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage[3]	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1.1	-1.7	-2.1	V
Drain-source on-resistance[3]	$R_{DS(on)}$	V_{GS} =-10V, I_D =-6A		26	33	mΩ
		V_{GS} =-4.5V, I_D =-5A		34	45	
Dynamic characteristics[4]						
Input Capacitance	C_{iss}	V_{DS} =-20V,V_{GS} =0V,f =1MHz		964		pF
Output Capacitance	C_{oss}			109		
Reverse Transfer Capacitance	C_{rss}			96		
Total Gate Charge	Q_g	V_{DS} =-20V,V_{GS} =-10V, I_D =-6A		22.9		nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			5.3		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-20V, V_{GS} =-10V, I_D =-6A, R_{GEN}=10Ω		5.5		nS
Turn-on rise time	t_r			14		
Turn-off delay time	$t_{d(off)}$			24		
Turn-off fall time	t_f			12		
Source-Drain Diode characteristics						
Diode Forward Current[2]	I_S				-6	A
Diode Forward voltage[3]	V_{SD}	V_{GS} =0V, I_S=-6A			-1.2	V

Notes:

1) Repetitive Rating: Pulse width limited by maximum junction temperature.
2) Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
3) Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4) Guaranteed by design, not subject to production.

Typical Characteristics

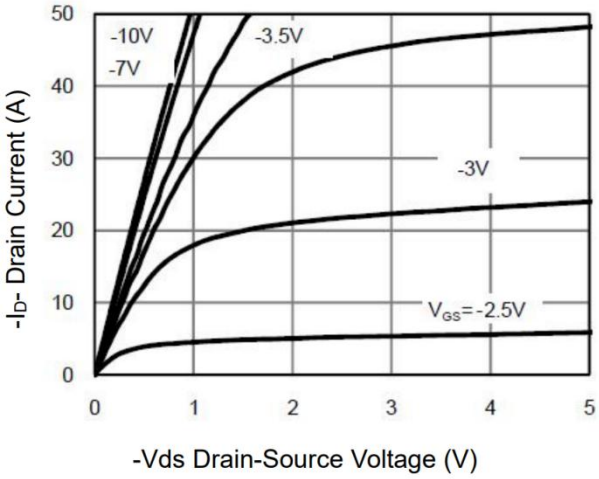


Figure 1 Output Characteristics

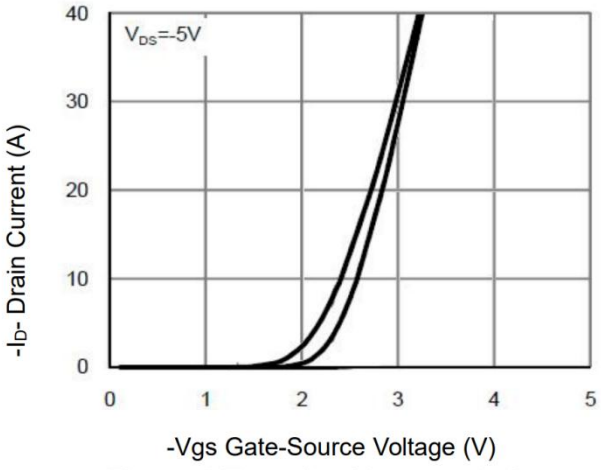


Figure 2 Transfer Characteristics

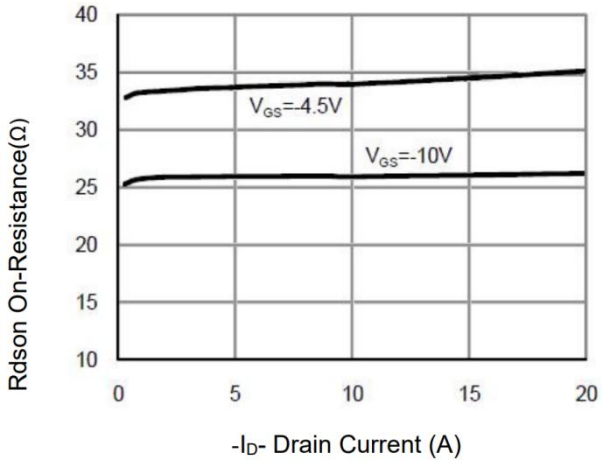


Figure 3 Rdson- Drain Current

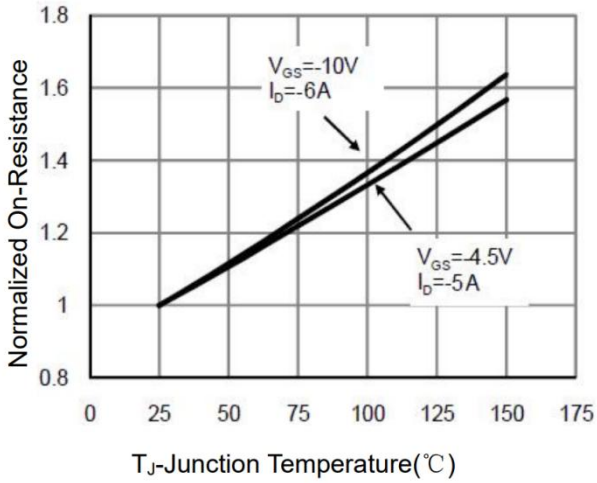


Figure 4 Rdson-Junction Temperature

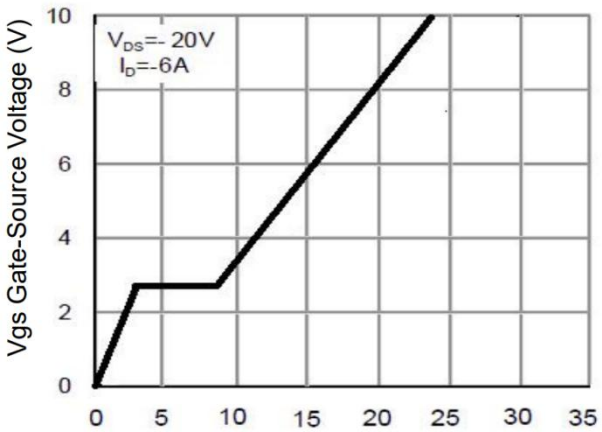


Figure 5 Gate Charge

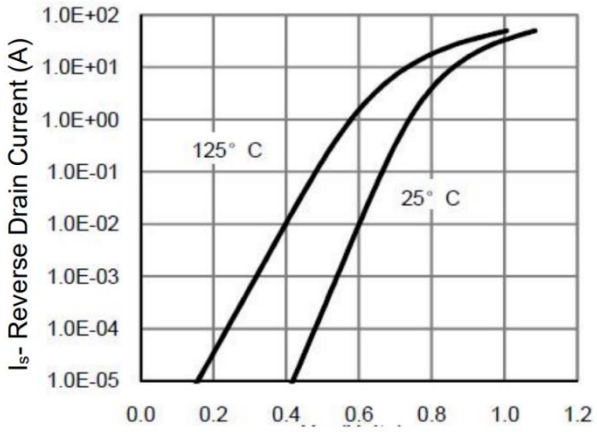


Figure 6 Source- Drain Diode Forward

Typical Characteristics

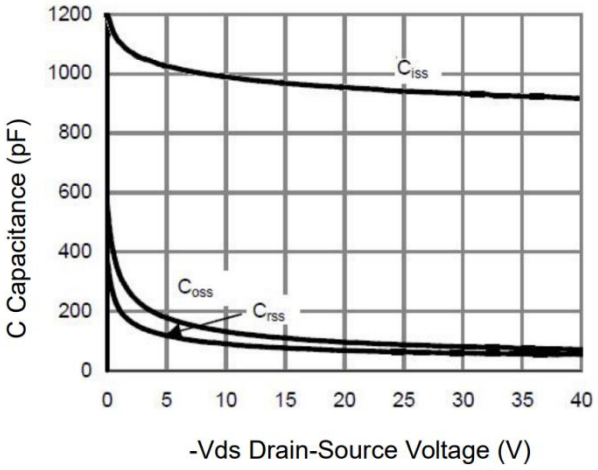


Figure 7 Capacitance vs Vds

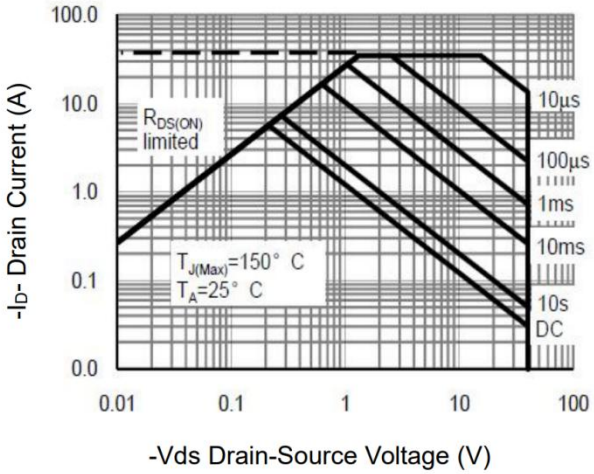


Figure 8 Safe Operation Area

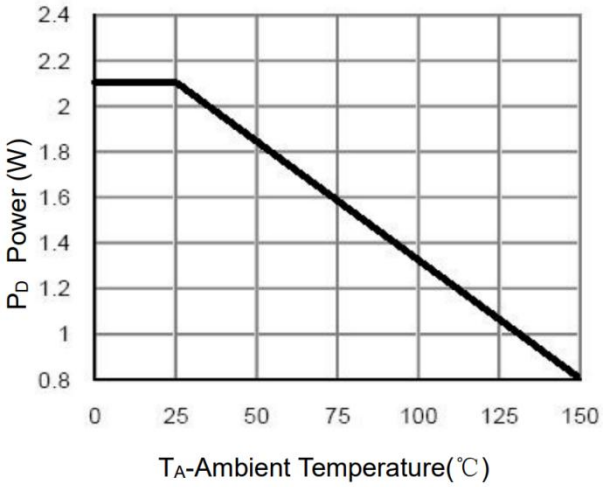


Figure 9 Power Dissipation

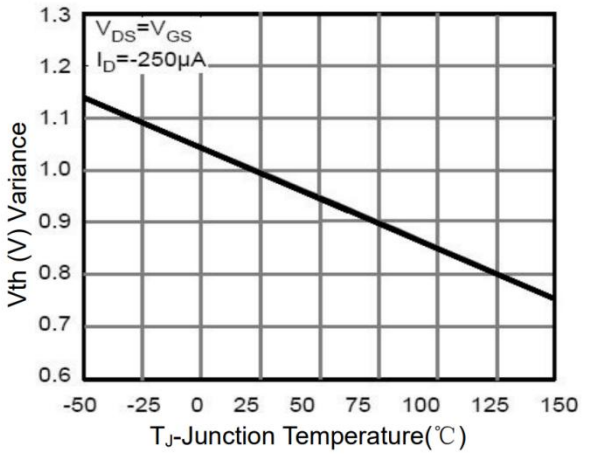


Figure 10 $V_{GS(th)}$ vs Junction Temperature

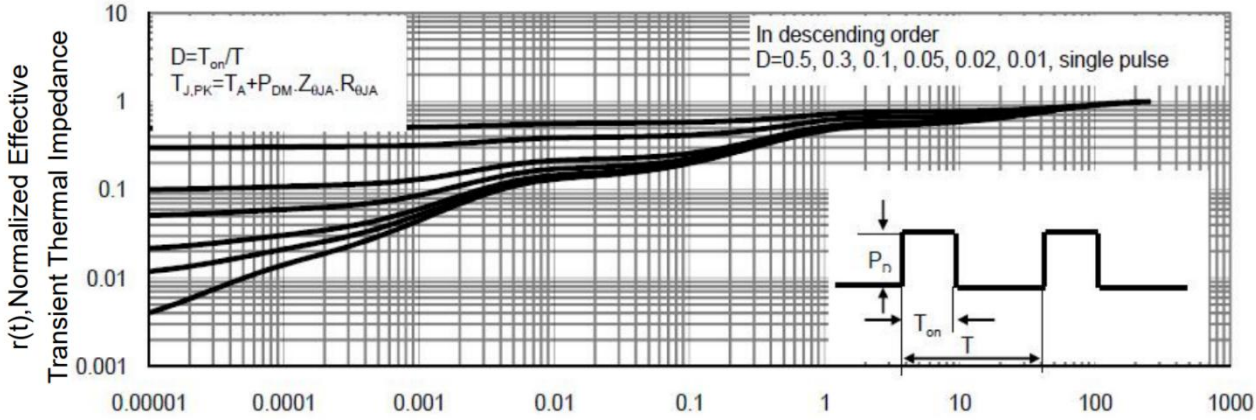
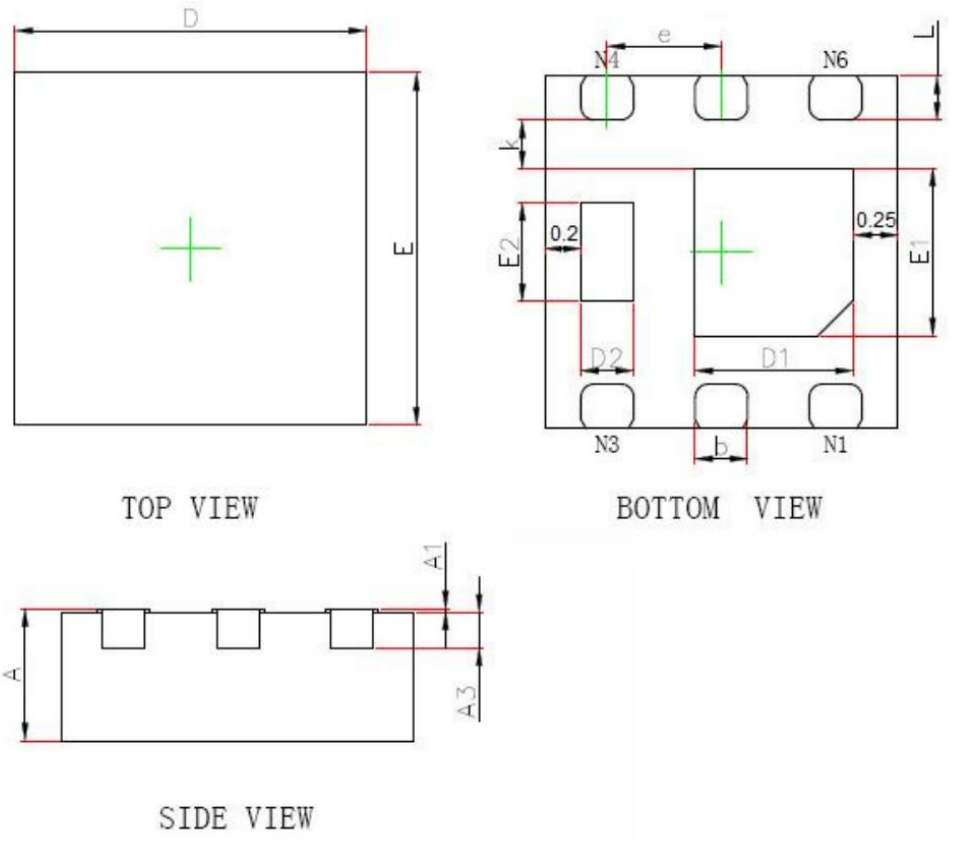


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN2*2-6L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.900	0.028	0.035
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	0.800	1.000	0.031	0.039
E1	0.850	1.050	0.033	0.041
D2	0.200	0.400	0.008	0.016
E2	0.460	0.660	0.018	0.026
k	0.200 MIN.		0.008 MIN.	
b	0.250	0.350	0.010	0.014
e	0.650 TYP.		0.026 TYP.	
L	0.174	0.326	0.007	0.013