AS15P03AS-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-30V	10mΩ@-10V	-15A
	15mΩ@-4.5V	

Feature

- High power and current handing capability
- Lead free product is acquired
- Surface mount package
- Suffix "-Q1" for AEC-Q101

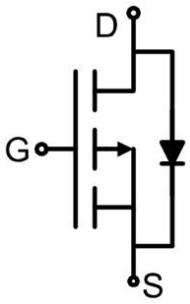
Application

- PWM applications
- Load switch
- Uninterruptible power supply

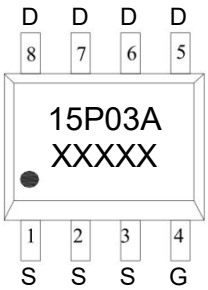
Package

SOP-8

Circuit diagram



Marking



AS15P03AS-Q1

P-Channel Enhancement Mode MOSFET

Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	-15	A
Pulsed Drain Current[1]	I_{DM}	-60	A
Avalanche energy[5]	E_{AS}	420	mJ
Power Dissipation	P_D	3.1	W
Thermal Resistance,Junction-to-Ambient[2]	$R_{\theta JA}$	40	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-30			V
Zero gate voltage drain current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate threshold voltage[3]	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-1.5	-2.2	V
Drain-source on-resistance[3]	$R_{DS(on)}$	V_{GS}=-10V, I_D=-15A		8.5	10	mΩ
		V_{GS}=-4.5V, I_D=-10A		11.5	15	
Dynamic characteristics[4]						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHz		2900		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			280		
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V,I_D=-10A		48		nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			14		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-15V,V_{GS}=-10V, I_D=-10A,R_{GEN}=3Ω		15		nS
Turn-on rise time	t_r			11		
Turn-off delay time	$t_{d(off)}$			44		
Turn-off fall time	t_f			21		
Source-Drain Diode characteristics						
Diode Forward voltage[3]	V_{SD}	V_{GS}=0V, I_S=-2A			-1.2	V

Notes:

1) Repetitive Rating: Pulse width limited by maximum junction temperature.

2) Surface Mounted on FR4 Board, t ≤ 10 sec. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

3) Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4) Guaranteed by design, not subject to production.

5) EAS condition: T_j=25℃,V_{DD}=-15V,V_G=-10V,L=0.5mH,R_g=25Ω.

Typical Characteristics

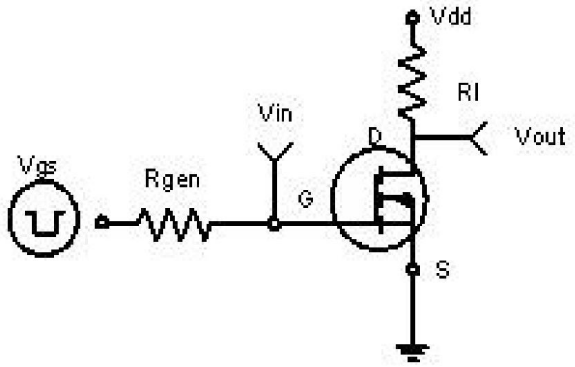


Figure 1 Switching Test Circuit

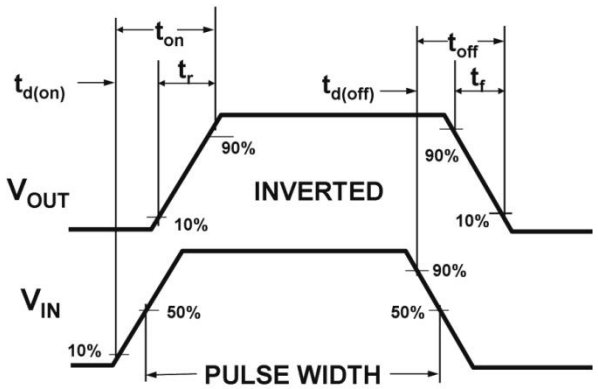


Figure 2 Switching Waveforms

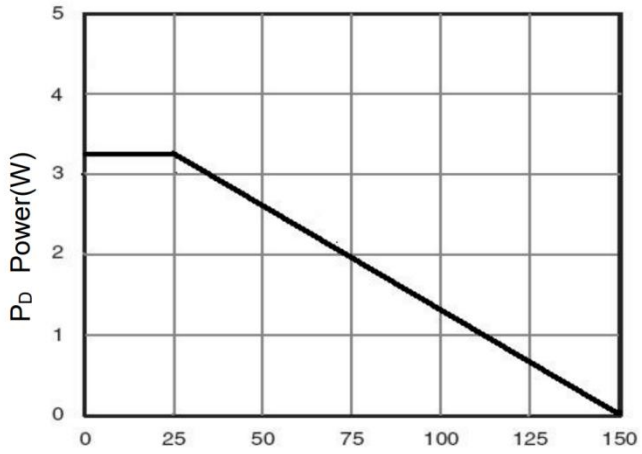


Figure 3 Power Dissipation

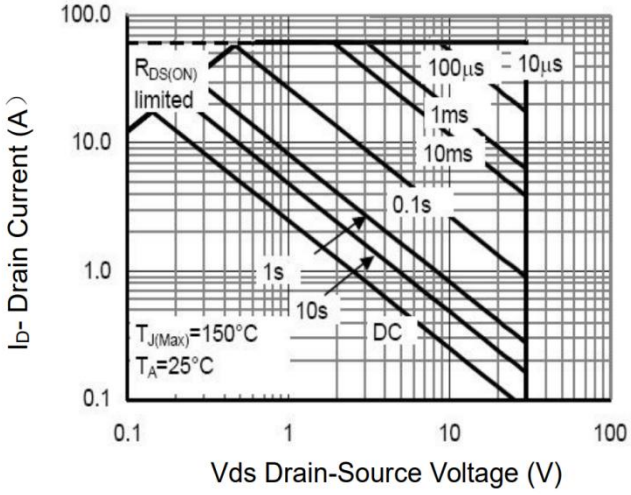


Figure 4 Safe Operation Area

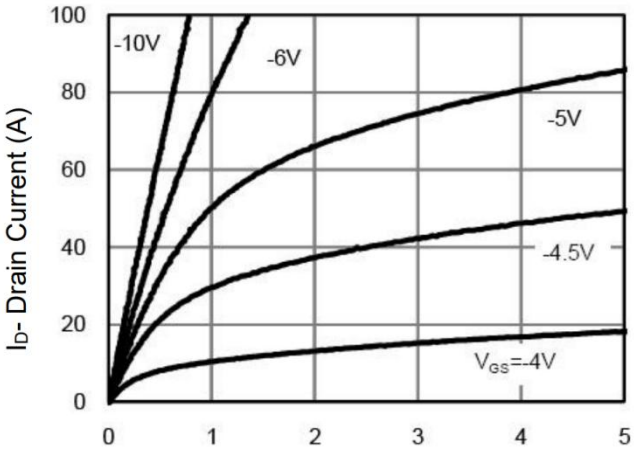


Figure 5 Output Characteristics

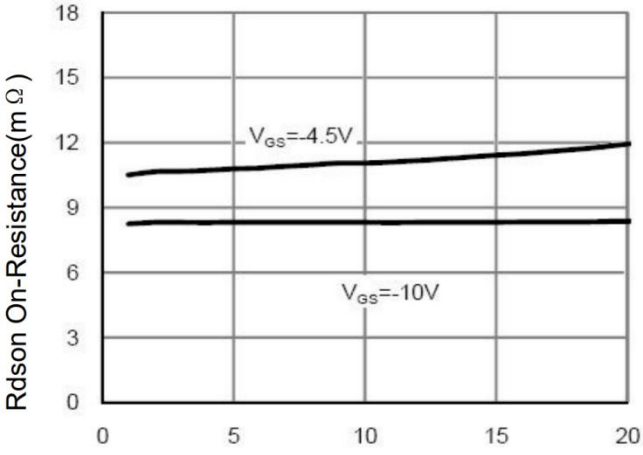


Figure 6 Drain-Source On-Resistance

Typical Characteristics

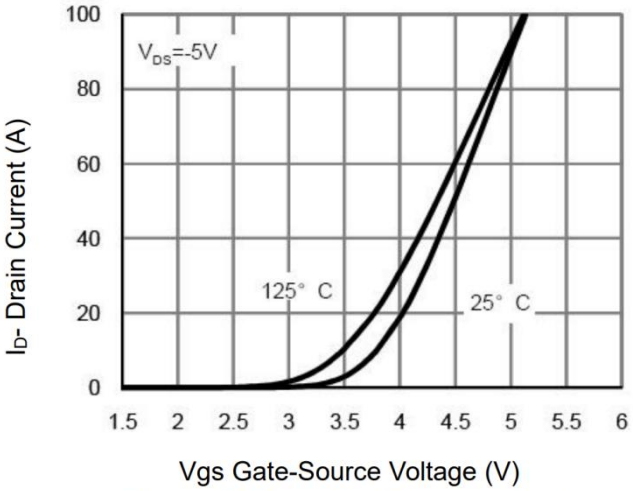


Figure 7 Transfer Characteristics

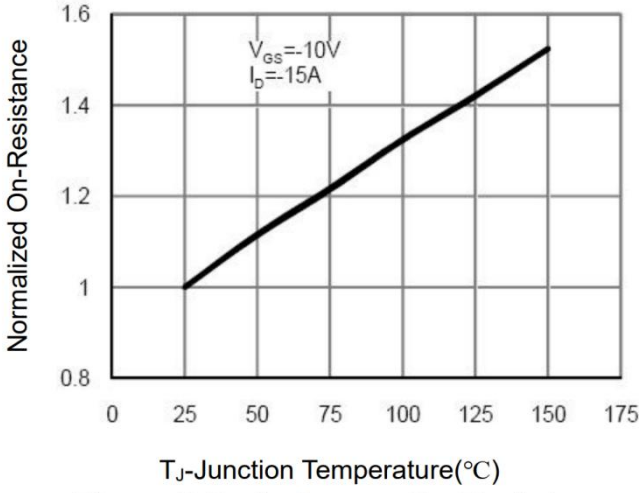


Figure 8 Drain-Source On-Resistance

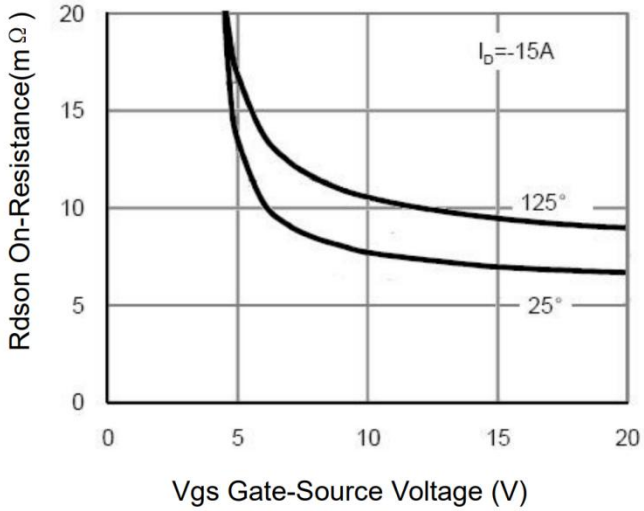


Figure 9 Rdson vs Vgs

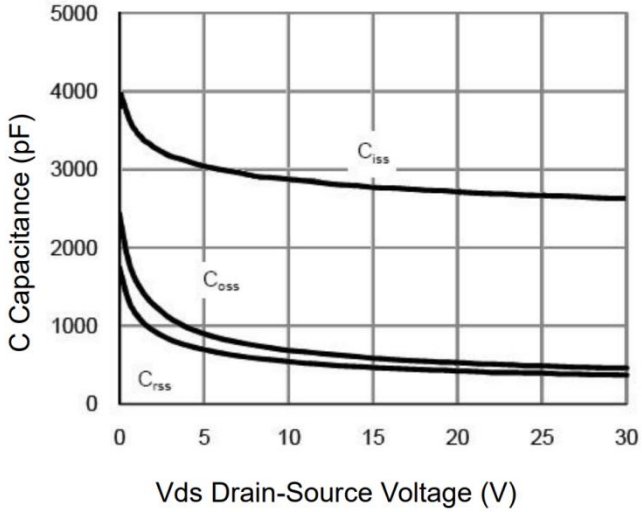


Figure 10 Capacitance vs Vds

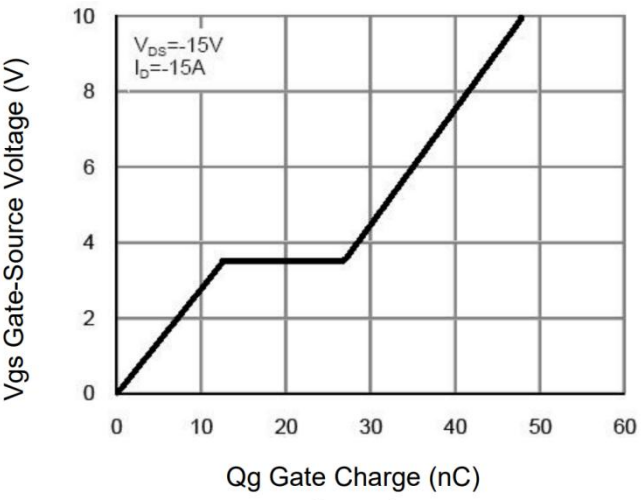


Figure 11 Gate Charge

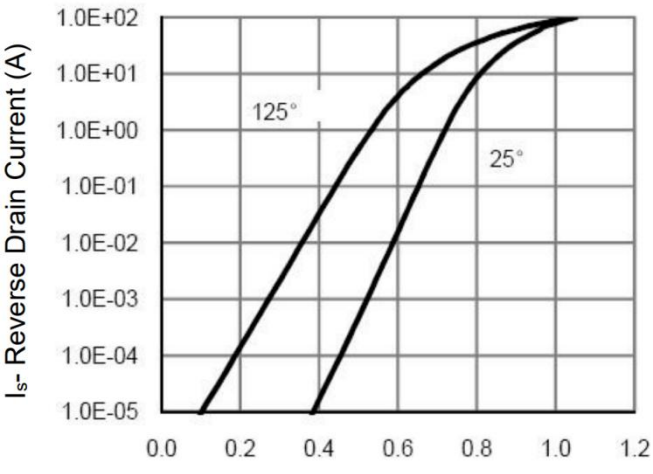


Figure 12 Source- Drain Diode Forward

Typical Characteristics

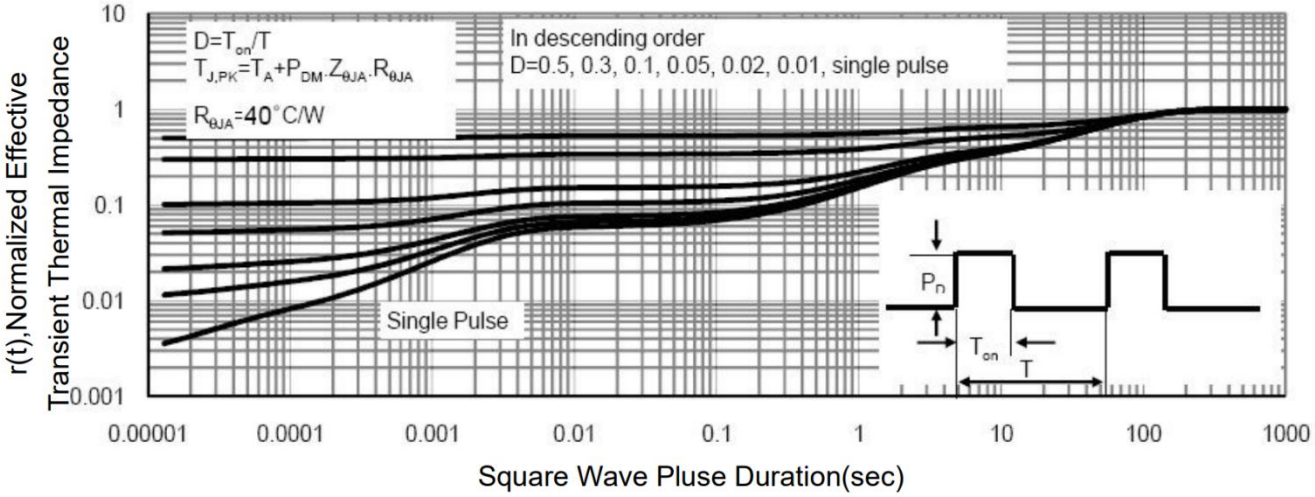
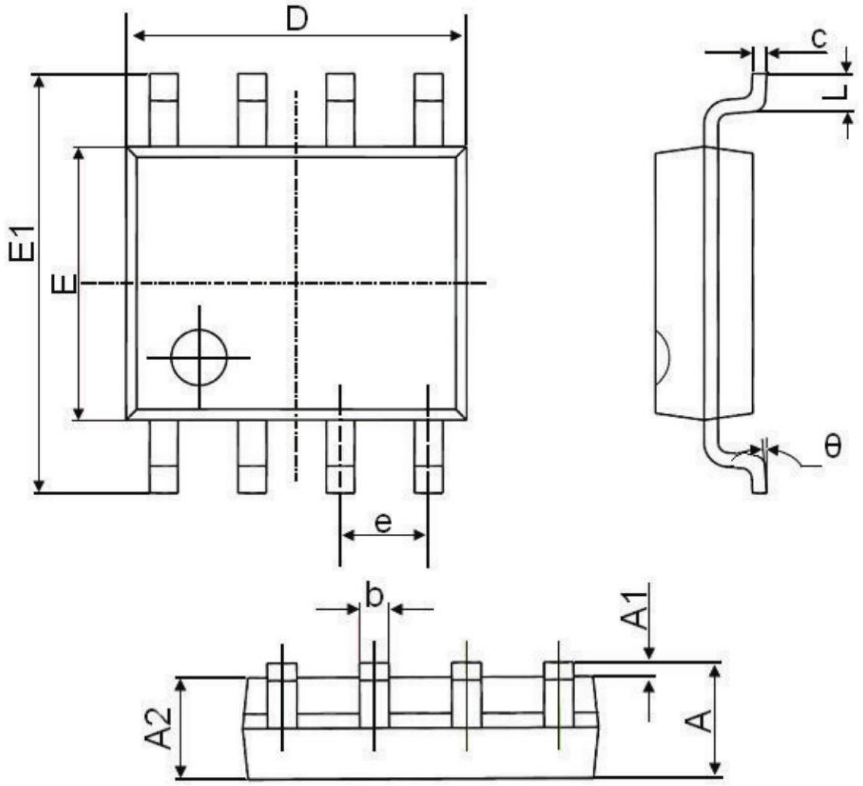


Figure 13 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°