

### Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_b$
-60V	50mΩ@-10V	-25A
	65mΩ@-4.5V	

### Feature

- High density cell design for low Rdson
- Split gate trench MOSFET technology
- Extremely low switching loss
- Excellent stability and uniformity
- Suffix "-Q1" for AEC-Q101

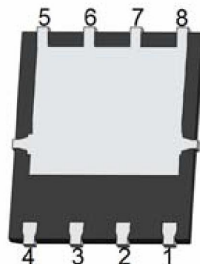
### Application

- Automotive Systems
- Industrial DC/DC Conversion Circuits

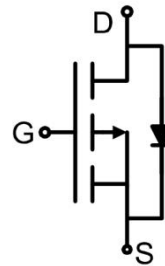
### Package



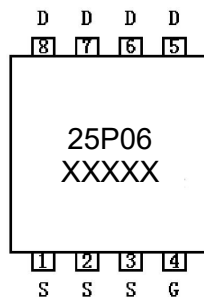
DFN5X6-8L



### Circuit diagram



### Marking



### Absolute maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	-60	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	-25	A
Pulsed Drain Current	I <sub>DM</sub>	-75	A
Power Dissipation	P <sub>D</sub>	60	W
Thermal Resistance,Junction-to-Ambient	R <sub>θJA</sub>	50	°C/W
Thermal Resistance,Junction-to-Case	R <sub>θJC</sub>	2.1	°C/W
Single pulse avalanche energy	E <sub>AS</sub>	81	mJ
Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ +150	°C

### Electrical characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-60			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V			-1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.3		-2.5	V
Drain-source on-resistance <sup>1)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -20A		38	50	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A		48	65	mΩ
<b>Dynamic characteristics<sup>2)</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1MHz		1100		pF
Output Capacitance	C <sub>oss</sub>			350		
Reverse Transfer Capacitance	C <sub>rss</sub>			28		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -20A		18.7		nC
Gate-Source Charge	Q <sub>gs</sub>			4.7		
Gate-Drain Charge	Q <sub>gd</sub>			3.0		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30V, V <sub>GS</sub> = -10V, R <sub>L</sub> = 2.5Ω, R <sub>GEN</sub> = 6Ω		7.5		nS
Turn-on rise time	t <sub>r</sub>			39.5		
Turn-off delay time	t <sub>d(off)</sub>			43.6		
Turn-off fall time	t <sub>f</sub>			55.1		
<b>Source-Drain Diode characteristics</b>						
Diode Forward Current <sup>1)</sup>	I <sub>S</sub>				-25	A
Diode Forward voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -20A			-1.3	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = -20A, di/dt = 100A/μs <sup>1)</sup>		20.2		nS
Reverse Recovery Charge	Q <sub>rr</sub>			8.2		nC

Notes:

1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.

2) Guaranteed by design, not subject to production testing.

## Typical Characteristics

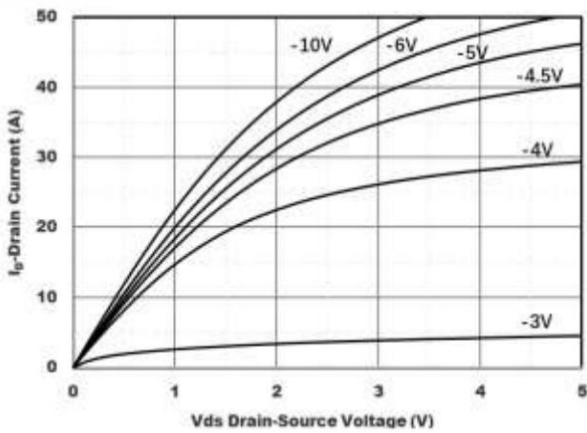


Figure1. Output Characteristics

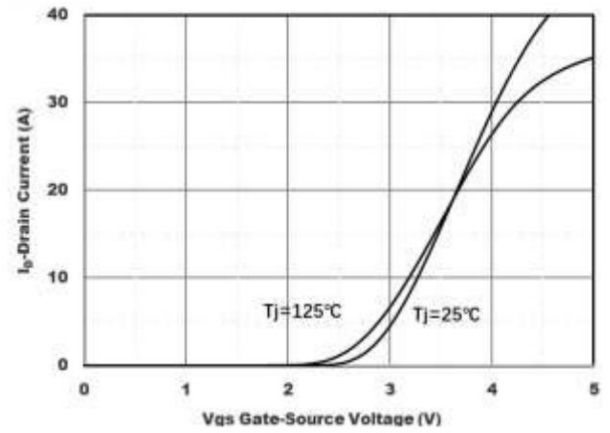


Figure2. Transfer Characteristics

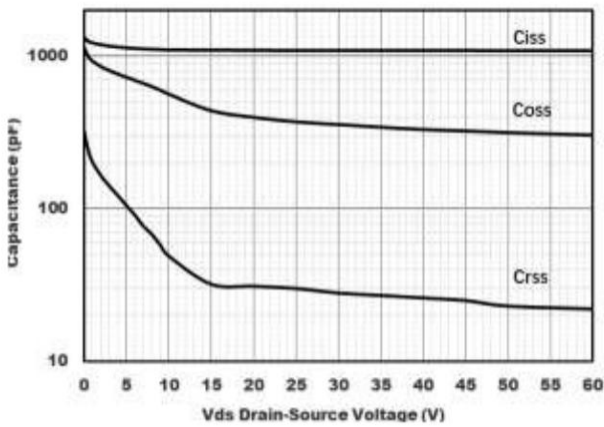


Figure3. Capacitance Characteristics

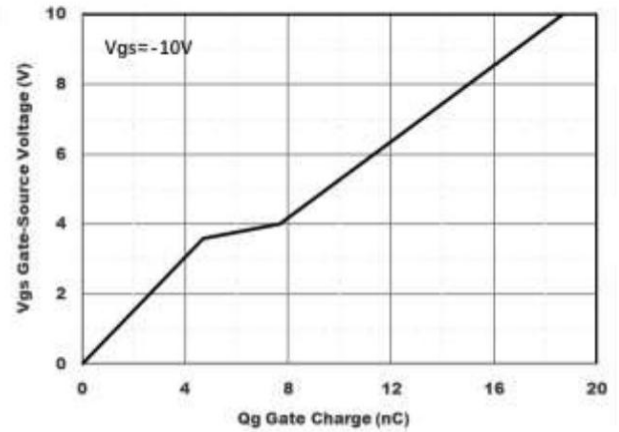


Figure4. Gate Charge

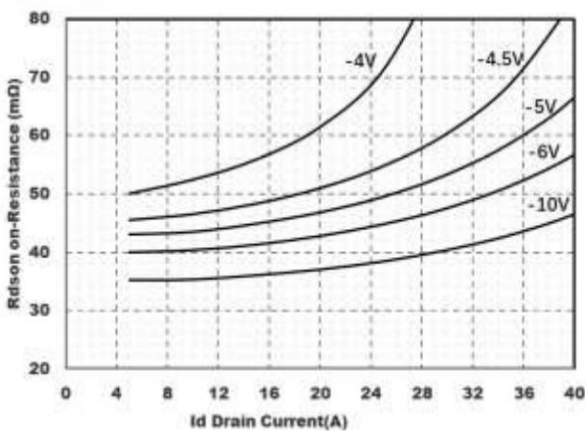


Figure5. : On-Resistance vs. Gate to Source Voltage

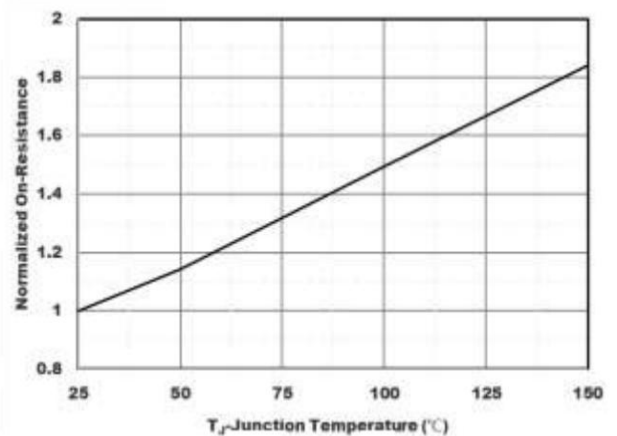


Figure6. Normalized On-Resistance

## Typical Characteristics

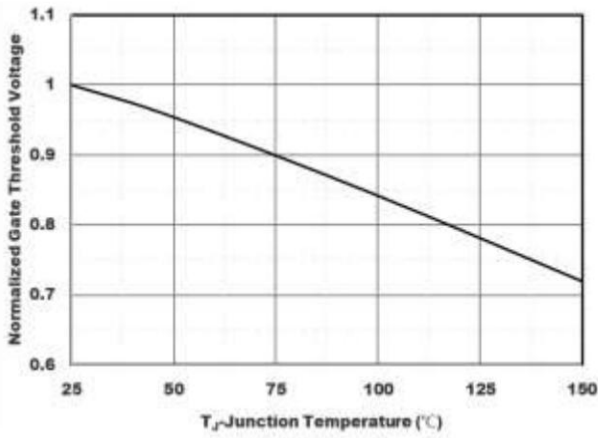


Figure 7. Normalized Gate Threshold Voltage

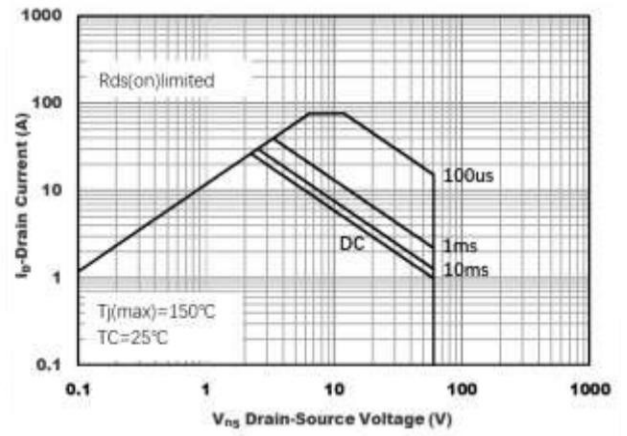


Figure 8. Safe Operation Area

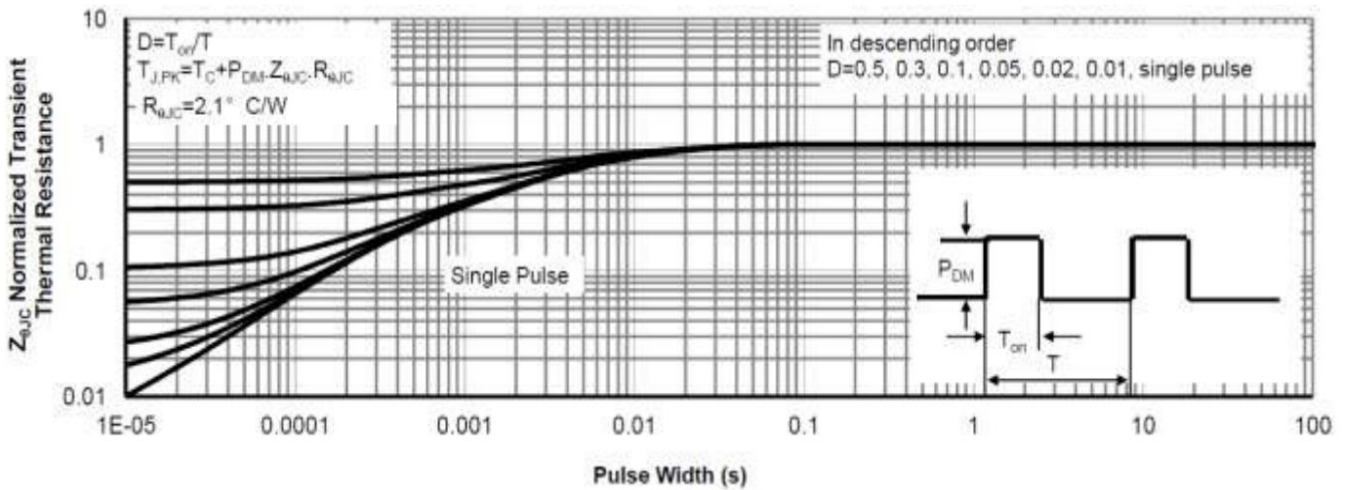
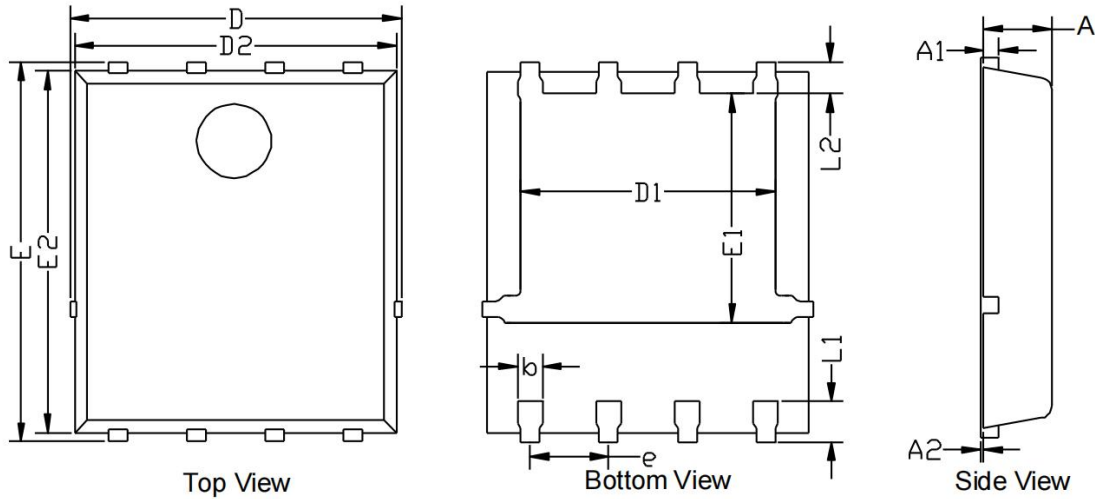


Figure 9. Normalized Maximum Transient thermal impedance

### DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.200	0.039	0.047
A1	0.254 BSC		0.010 BSC	
A2	0.000	0.100	0.000	0.004
D	5.150	5.550	0.203	0.219
E	5.950	6.350	0.234	0.250
D1	3.910	4.320	0.154	0.170
E1	3.520	3.920	0.139	0.154
D2	5.000	5.400	0.197	0.213
E2	5.660	6.060	0.223	0.239
b	0.310	0.510	0.012	0.020
e	1.270 BSC		0.050 BSC	
L1	0.560	0.760	0.022	0.030
L2	0.500 BSC		0.020 BSC	