AS3139EN-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-20V	850mΩ@-4.5V	-0.65A
	1200mΩ@-2.5V	
	2000mΩ@-1.8V	

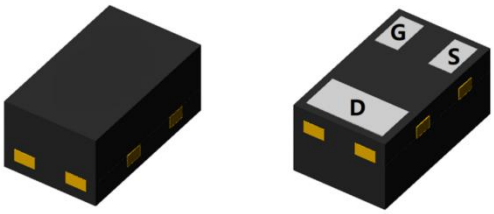
Feature

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- ESD Protected Up to 2.0KV(HBM)
- Suffix "-Q1" for AEC-Q101

Application

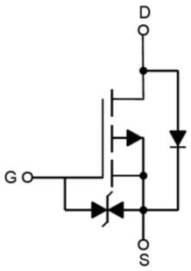
- Interfacing, Logic switch
- Load switch
- Power management

Package



DFN1006-3L

Circuit diagram



Marking

9A

Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	-0.65	A
Continuous Drain Current (T_A=70℃)	I_D	-0.52	A
Pulsed Drain Current[1)]	I_{DM}	-2	A
Power Dissipation	P_D	0.9	W
Thermal Resistance from Junction to Ambient[2)]	$R_{\theta JA}$	138	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V,V_{GS} = 0V,T_C=25℃			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±10	μA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.35	-0.62	-1.2	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-0.5A		580	850	mΩ
		V_{GS} =-2.5V, I_D =-0.3A		855	1200	
		V_{GS} =-1.8V, I_D =-0.2A		1350	2000	
Dynamic characteristics[3)]						
Input Capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		71		pF
Output Capacitance	C_{oss}			20		
Reverse Transfer Capacitance	C_{rss}			15		
Total Gate Charge	Q_g	V_{DD} =-10V,V_{GS} =-4.5V, I_D =-0.5A		1.24		nC
Gate-Source Charge	Q_{gs}			0.37		
Gate-Drain Charge	Q_{gd}			0.27		
Turn-on delay time	$t_{d(on)}$	V_{DD} =-10V, V_{GS} =-4.5V, R_L =2.5Ω, R_{GEN}=3Ω		4		nS
Turn-on rise time	t_r			19		
Turn-off delay time	$t_{d(off)}$			16		
Turn-off fall time	t_f			25		
Source-Drain Diode characteristics						
Diode Forward Current	I_S				-0.65	A
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S=-0.65A			-1.2	V
Reverse Recovery Time	t_{rr}	I_F =-0.5A, di/dt =-20A/μs		26		nS
Reverse Recovery Charge	Q_{rr}			0.97		nC

Notes:

1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

2) The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_D is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

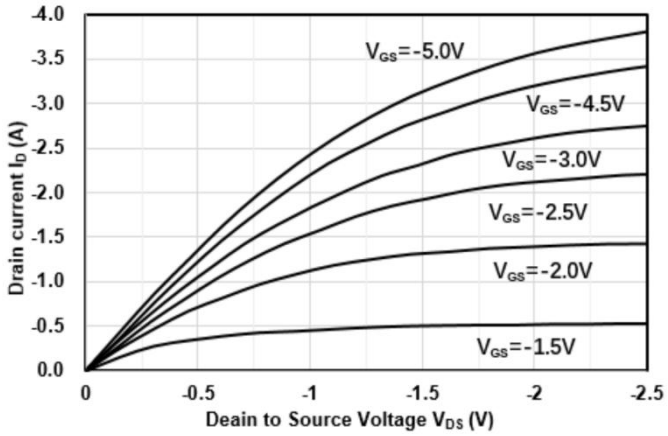


Figure1. Output Characteristics

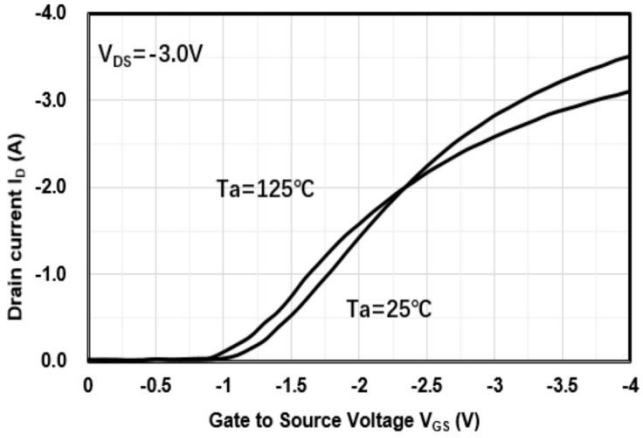


Figure2. Transfer Characteristics

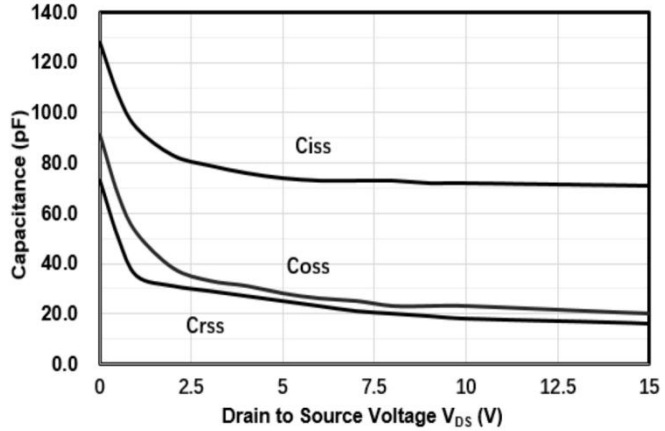


Figure3. Capacitance Characteristics

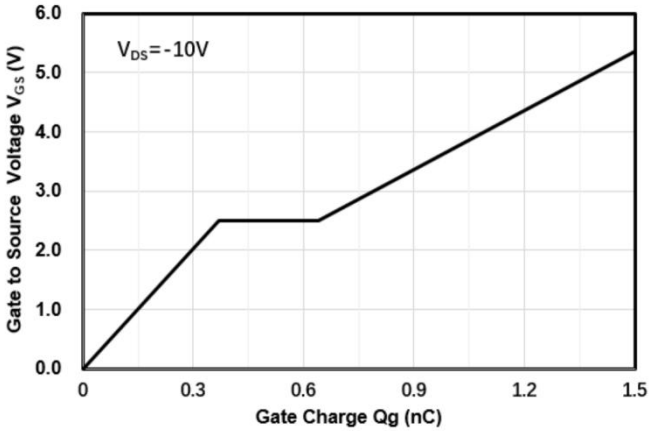


Figure4. Gate Charge

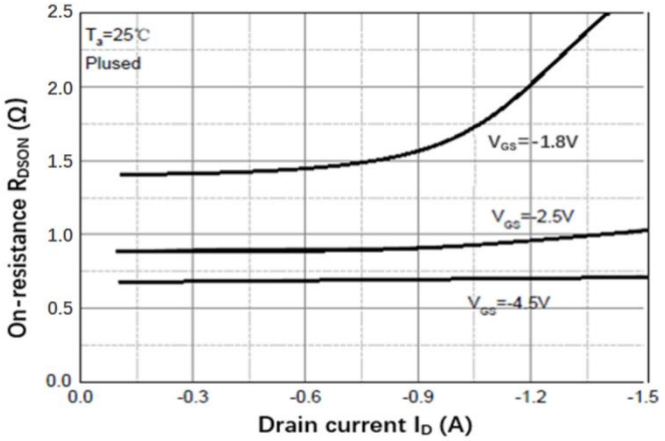


Figure5. Drain-Source on Resistance

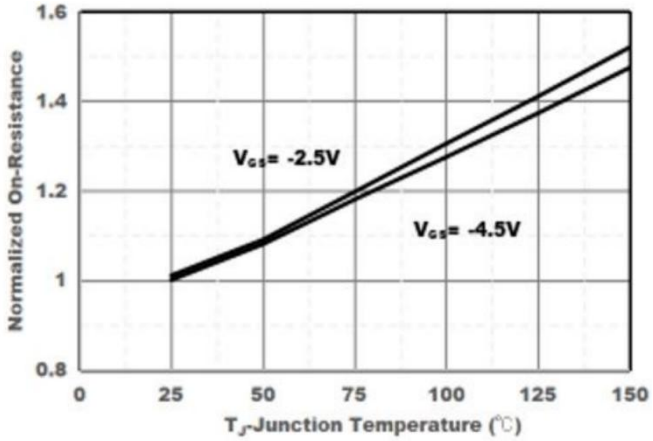


Figure6. Drain-Source on Resistance

Typical Characteristics

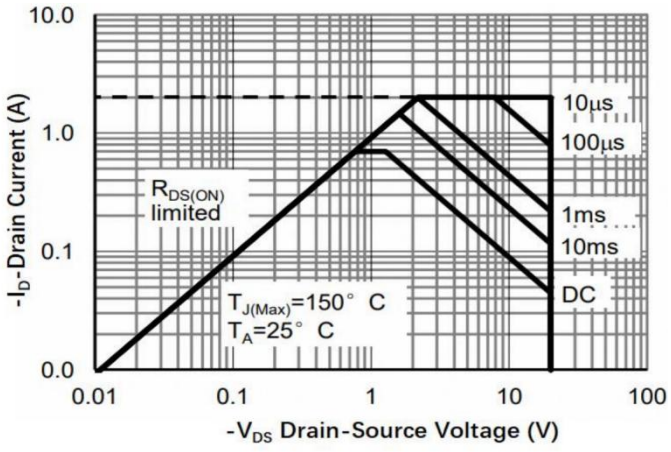


Figure7. Safe Operation Area

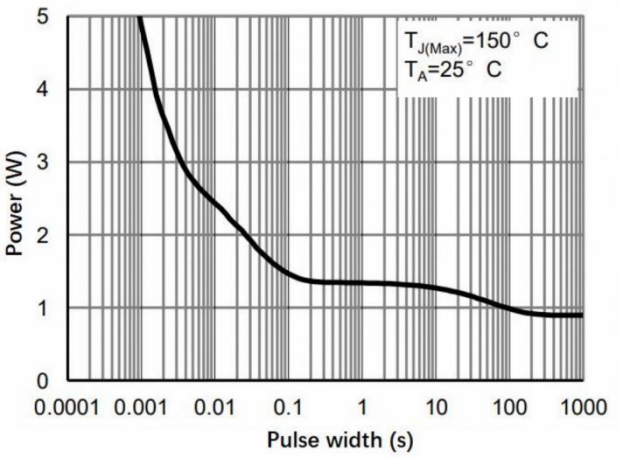


Figure8. Pulse Power Rating Junction-to-Ambient

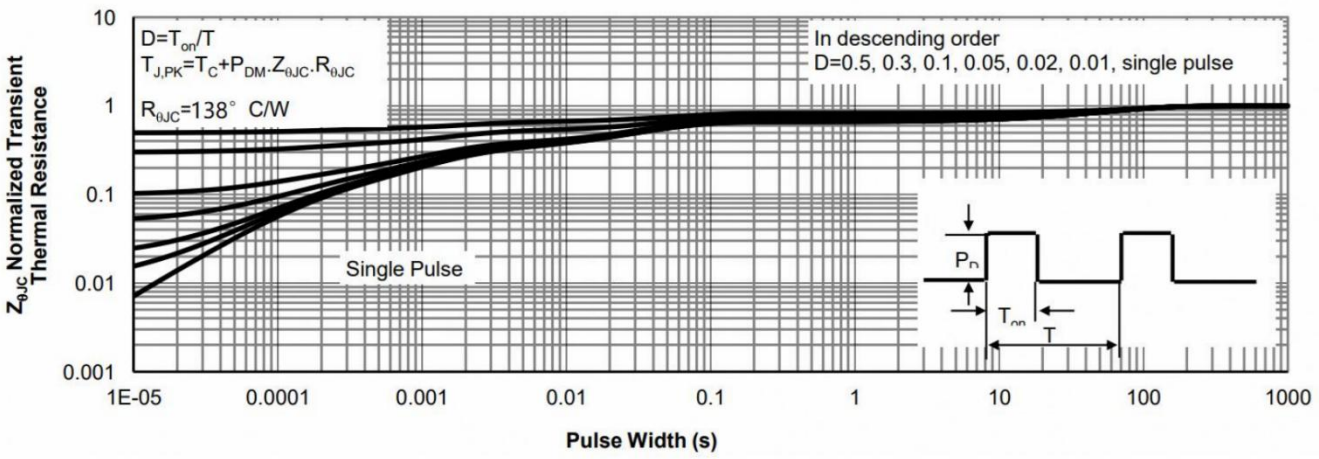
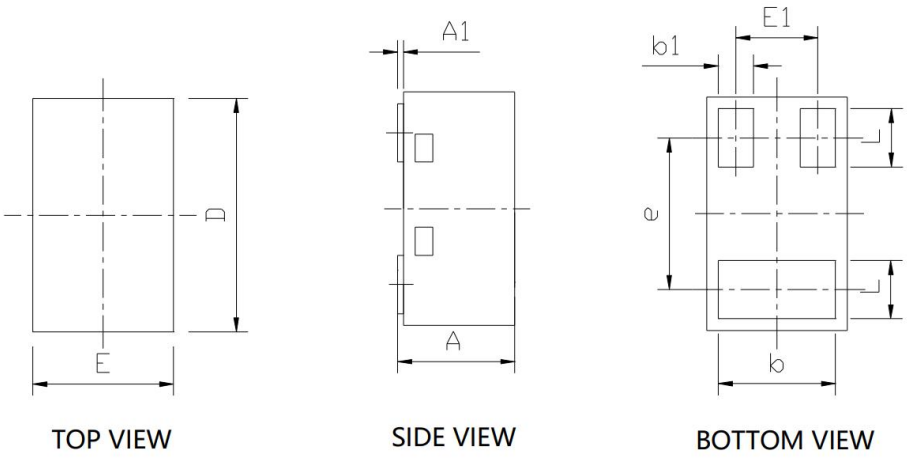


Figure9. Normalized Maximum Transient Thermal Impedance

DFN1006-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.420	0.550	0.017	0.022
A1	0.025 REF		0.001 REF	
b	0.450	0.550	0.018	0.022
b1	0.100	0.200	0.004	0.008
D	0.950	1.050	0.037	0.041
E	0.550	0.650	0.022	0.026
E1	0.350 BSC		0.014 BSC	
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012