

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$
-30V	23mΩ@-10V	-11A
	36mΩ@-4.5V	

## Feature

- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Suffix "-Q1" for AEC-Q101

## Application

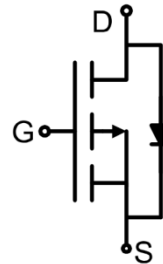
- Load Switch
- Battery Switch
- Power management

## Package



SOP-8

## Circuit diagram



## Marking



### Absolute maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	-11	A
Pulsed Drain Current	$I_{DM}$	-50	A
Power Dissipation	$P_D$	3.0	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40	$^{\circ}C/W$
Junction Temperature	$T_J$	150	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^{\circ}C$

### Electrical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$			-1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 100$	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1		-3	V
Drain-source on-resistance <sup>1)</sup>	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$		16	23	m $\Omega$
		$V_{GS} = -4.5V, I_D = -5A$		21	36	
<b>Dynamic characteristics<sup>2)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$		1130		pF
Output Capacitance	$C_{oss}$			240		
Reverse Transfer Capacitance	$C_{rss}$			155		
Total Gate Charge	$Q_g$	$V_{DS} = -15V, V_{GS} = -10V, I_D = -10A$		18		nC
Gate-Source Charge	$Q_{gs}$			5.5		
Gate-Drain Charge	$Q_{gd}$			3.3		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15V, V_{GS} = -10V, I_D = -1A, R_{GEN} = 3\Omega$		8.7		nS
Turn-on rise time	$t_r$			8.5		
Turn-off delay time	$t_{d(off)}$			18		
Turn-off fall time	$t_f$			7		
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage	$V_{DS}$	$V_{GS} = 0V, I_S = -2.1A$			-1.2	V

Notes:

- 1) Pulse Test: Pulse Width < 300 $\mu s$ , Duty Cycle  $\leq 2\%$ .
- 2) Guaranteed by design, not subject to production testing.

## Typical Characteristics

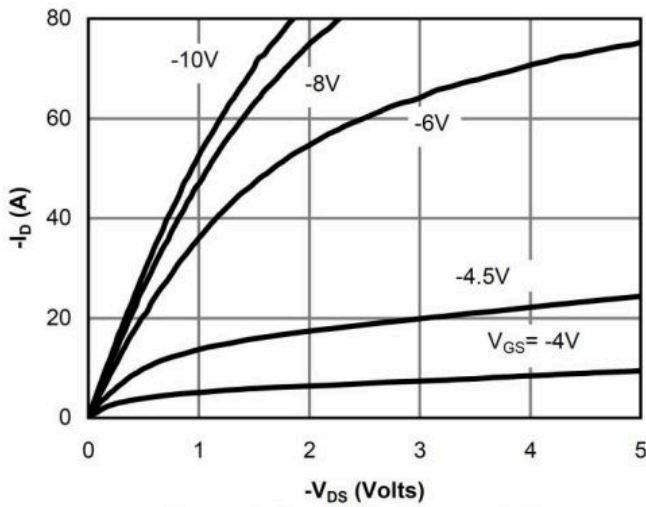


Figure 1: On-Region Characteristics

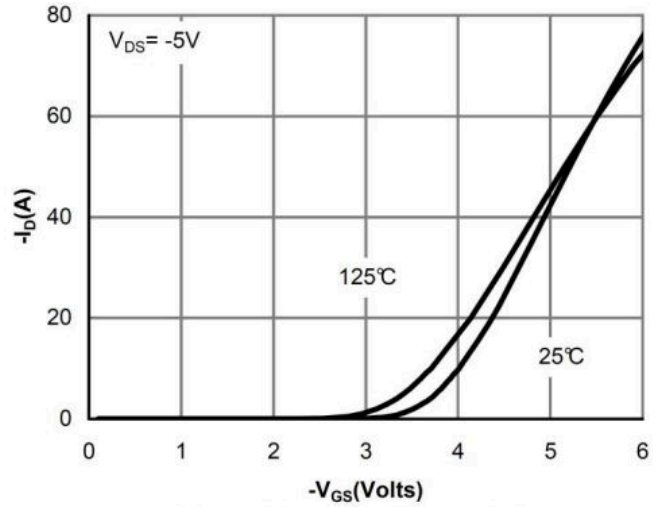


Figure 2: Transfer Characteristics

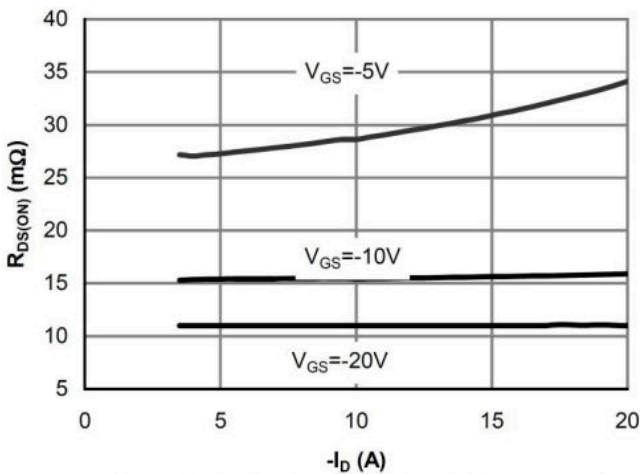


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

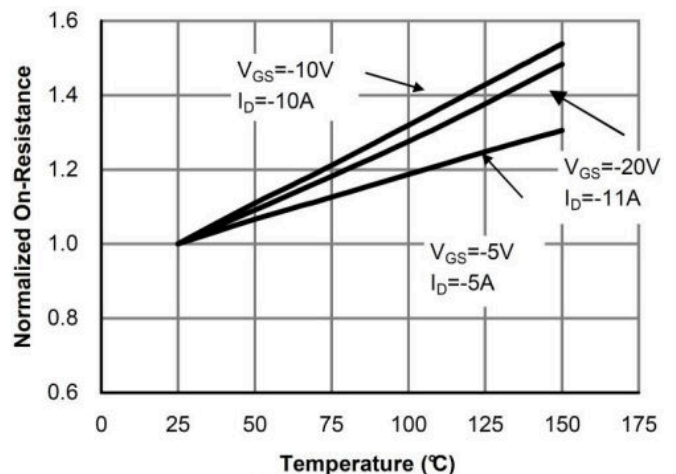


Figure 4: On-Resistance vs. Junction Temperature

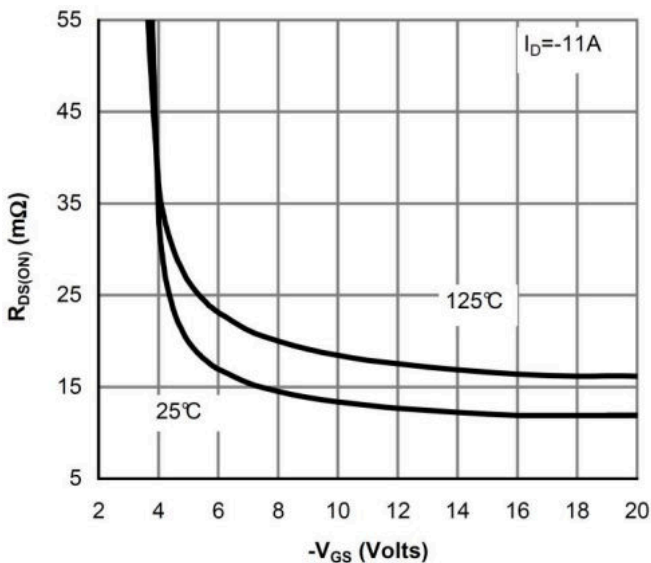


Figure 5: On-Resistance vs. Gate-Source Voltage

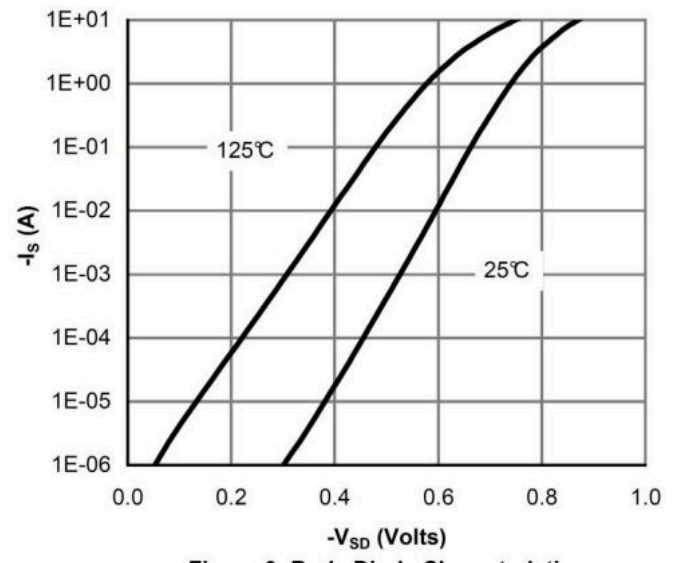


Figure 6: Body-Diode Characteristics

## Typical Characteristics

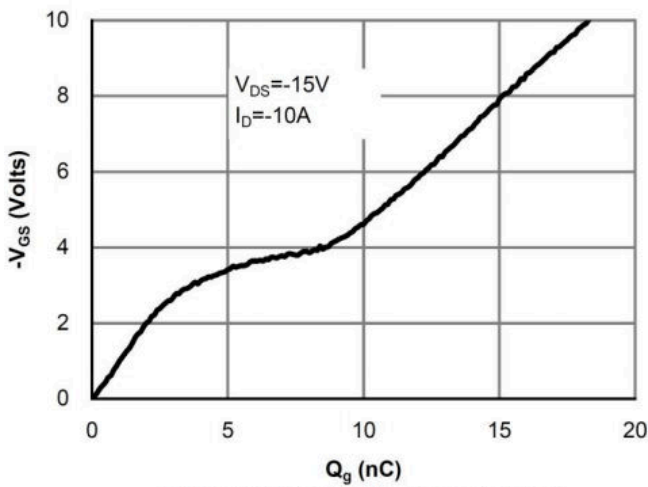


Figure 7: Gate-Charge Characteristics

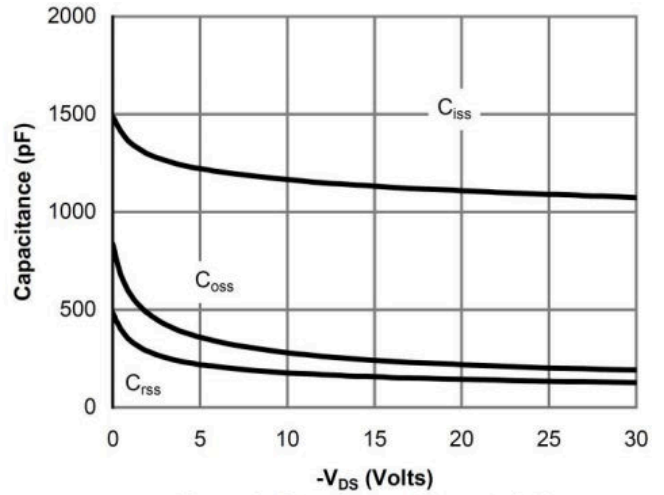


Figure 8: Capacitance Characteristics

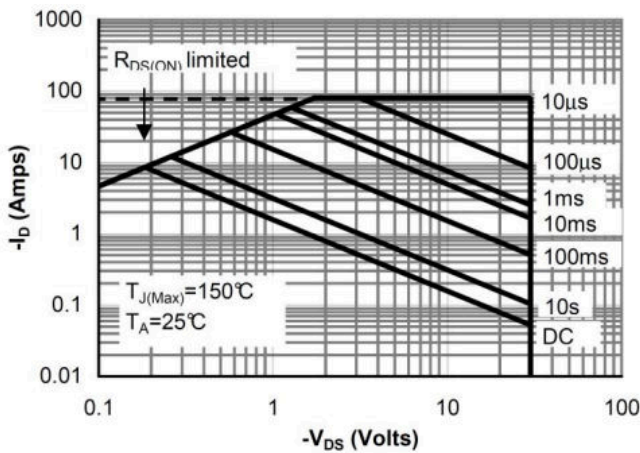


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

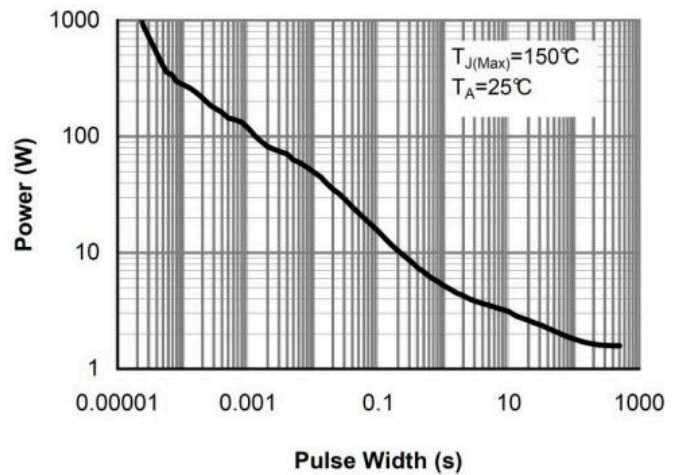


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

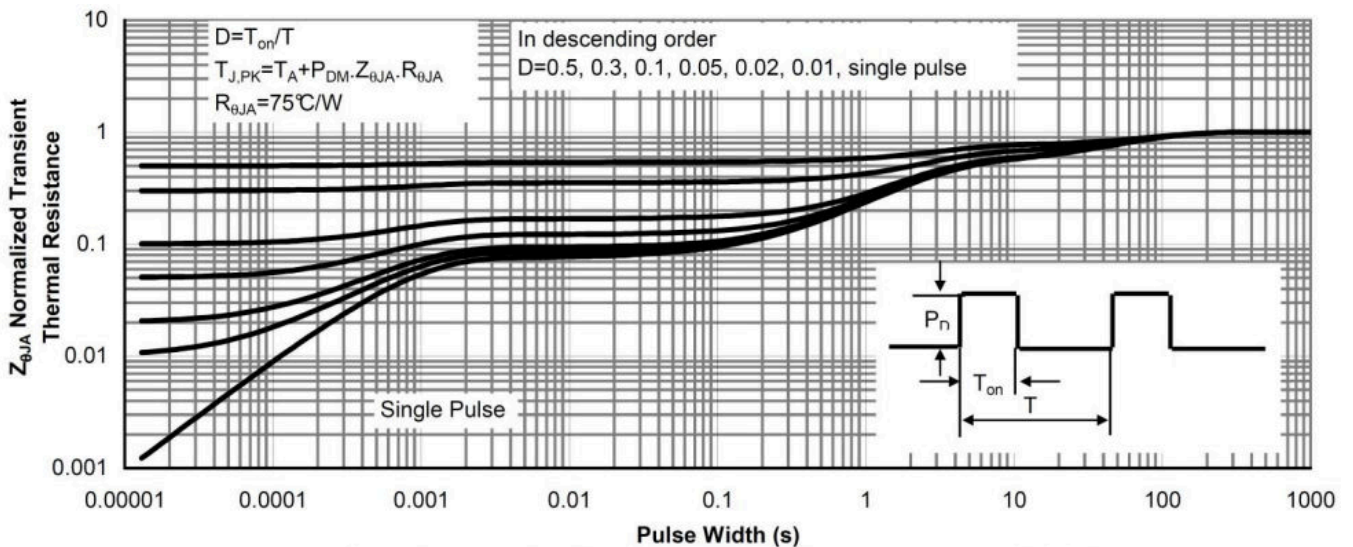
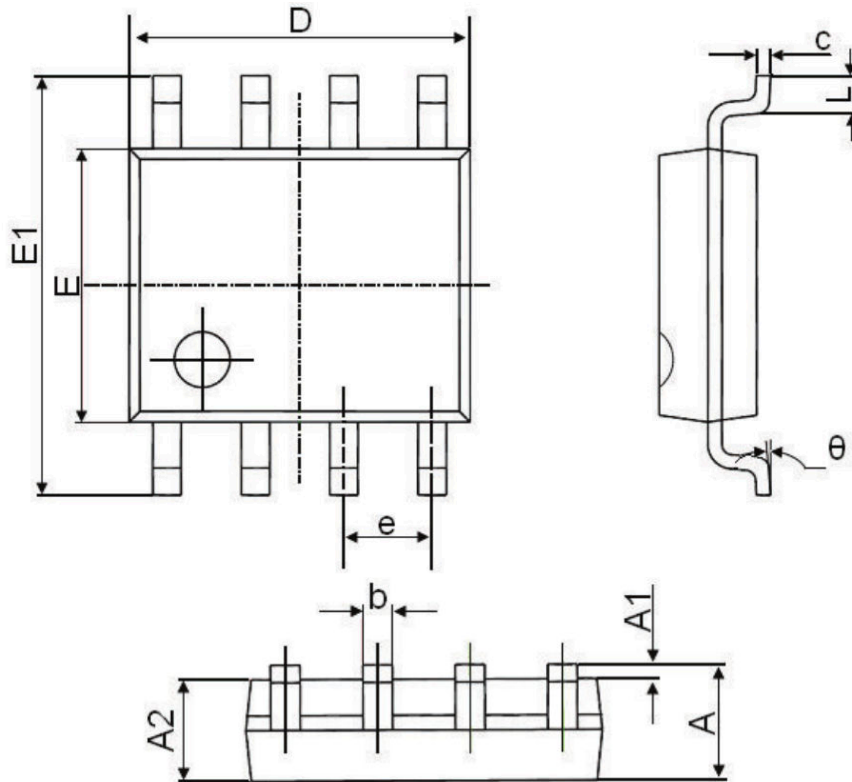


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

## SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°