AS8810ETS

Dual N-Channel MOSFET ESD Protection

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
20V	16mΩ@10V	6.5A
	18mΩ@4.5V	
	24mΩ@2.5V	

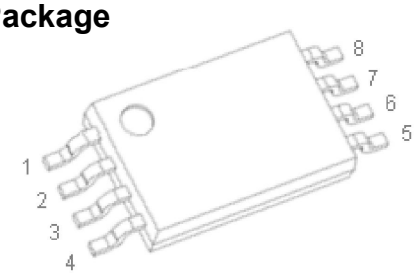
Feature

- Super high dense cell trench design for low $R_{DS(on)}$
- Rugged and reliable
- Surface mount package
- ESD protected 2KV

Application

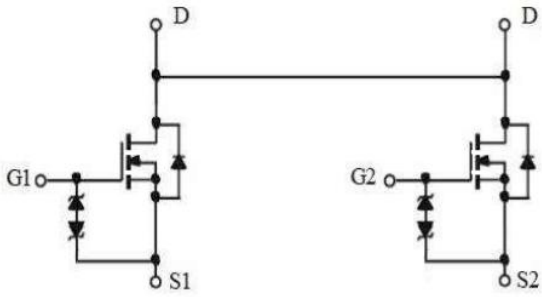
- Battery switch

Package

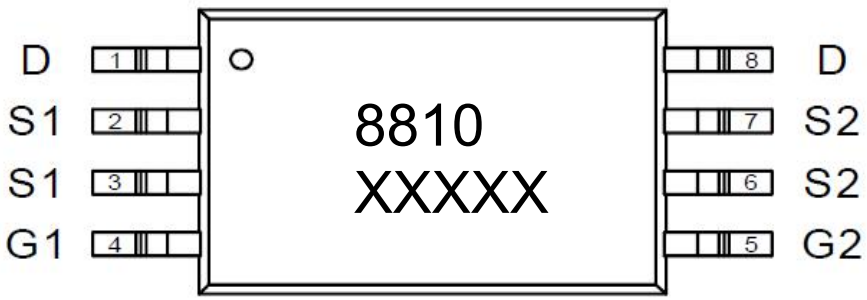


TSSOP-8

Circuit diagram



Marking



Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current[1)]	I_D	6.5	A
Pulsed Drain Current[2)]	I_{DM}	30	A
Power Dissipation	P_D	1.5	W
Thermal Resistance from Junction to Ambient[1)]	$R_{\theta JA}$	83	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_j=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =16V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±10	μA
Gate threshold voltage[3)]	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.6	0.8	1.0	V
Drain-source on-resistance[3)]	$R_{DS(on)}$	V_{GS} =10V, I_D =6.5A		13	16	mΩ
		V_{GS} =5.5V, I_D =4A			17.5	
		V_{GS} =4.5V, I_D =6.5A		15	18	
		V_{GS} =2.5V, I_D =6A		19.5	24	
Forward transconductance[3)]	g_{FS}	V_{DS} =10V,I_D =6.5A		19		S
Dynamic characteristics[3)]						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		318		pF
Output Capacitance	C_{oss}			103		
Reverse Transfer Capacitance	C_{rss}			22		
Total Gate Charge	Q_g	V_{DS} =12V,V_{GS} =4.5V,I_D =6A		4.6		nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-on delay time	$t_{d(on)}$	V_{DS}=10V,V_{GS}=4.5V,I_D =2A R_{GEN}=6Ω,R_L=5Ω		304		nS
Turn-on rise time	t_r			720		
Turn-off delay time	$t_{d(off)}$			3480		
Turn-off fall time	t_f			2140		
Source-Drain Diode characteristics						
Diode Forward voltage[3)]	V_{SD}	V_{GS} =0V, I_S=1.5A			1.2	V

Notes:

1) Surface mounted on FR4 Board, t ≤ 10sec.

2) Pulse test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

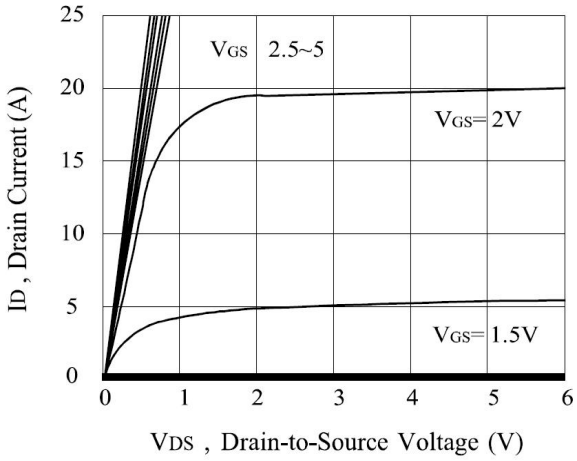


Figure 1. Output Characteristics

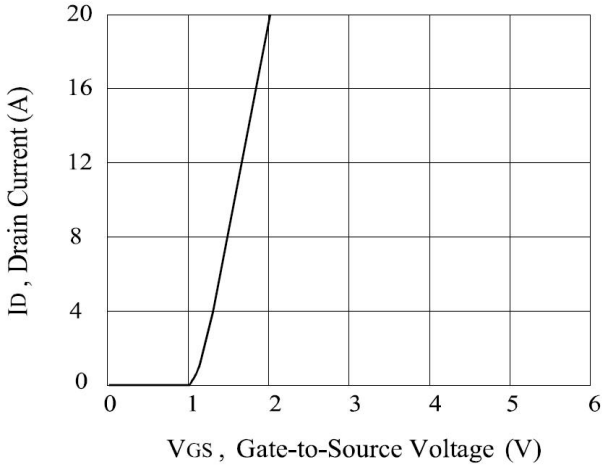


Figure 2. Transfer Characteristics

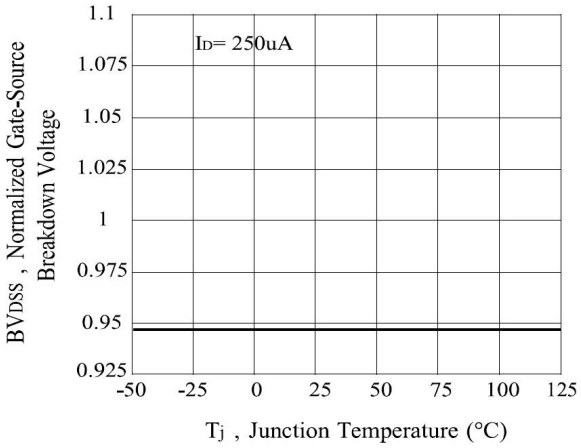


Figure 3. Breakdown Voltage Variation with Temperature

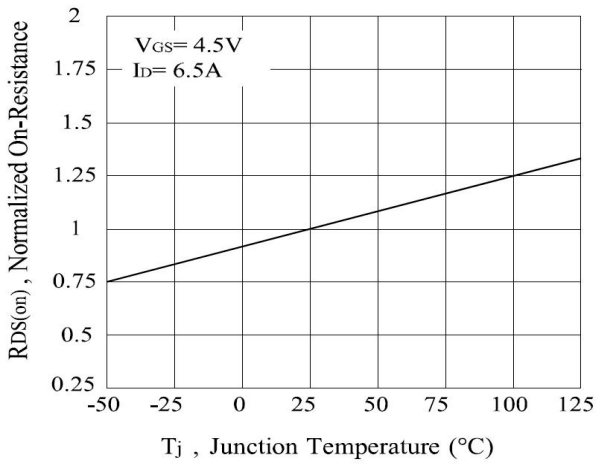


Figure 4. On-Resistance Variation with Temperature

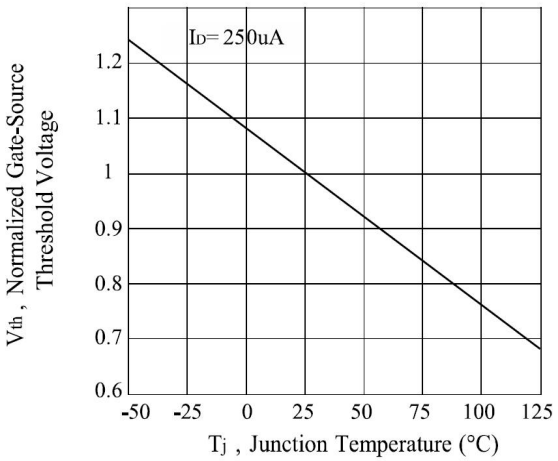


Figure 5. Gate Threshold Variation with Temperature

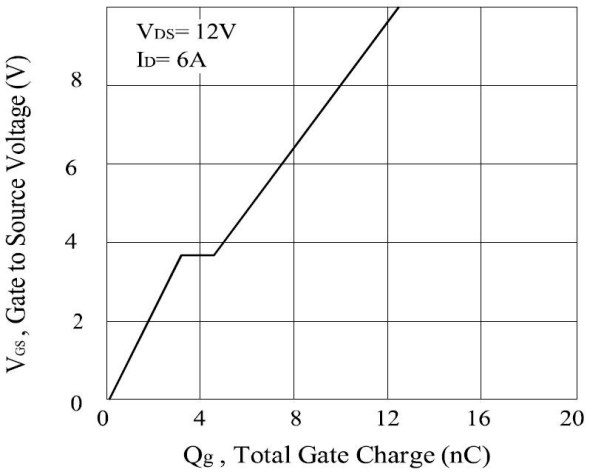
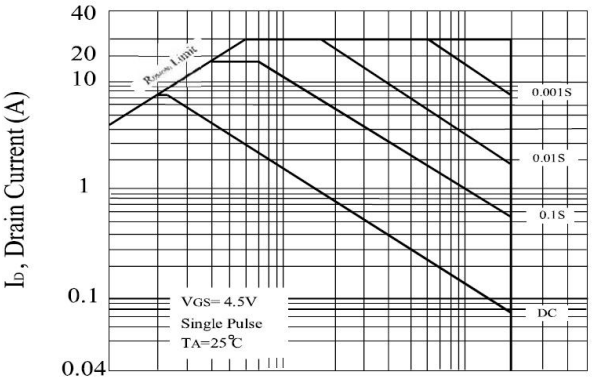


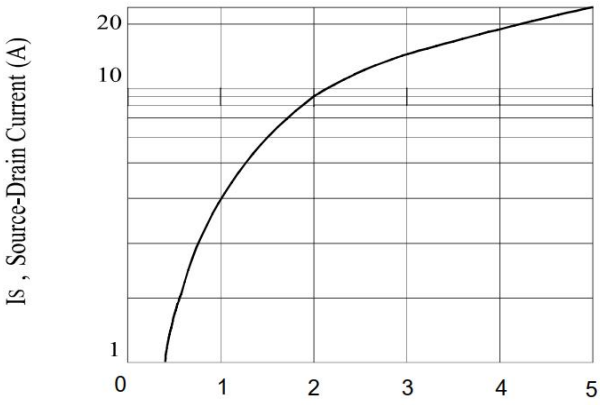
Figure 6. Gate Charge

Typical Characteristics



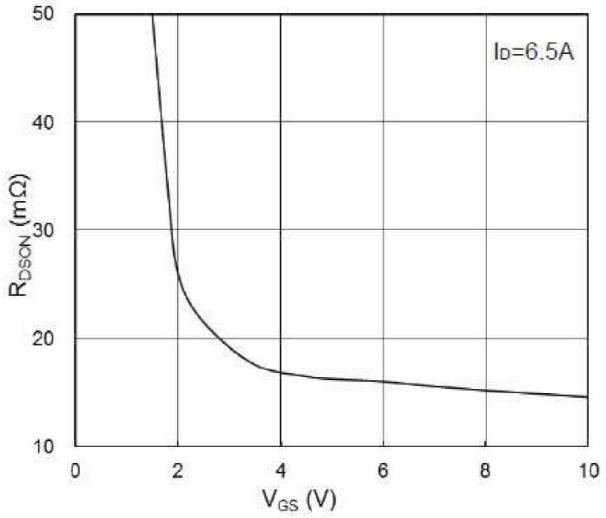
VDS , Drain-Source Voltage (V)

Figure 7. Maximum Safe Operating Area



VSD , Body Diode Forward Voltage (V)

Figure 8. Body Diode Forward Voltage Variatic with Source Current



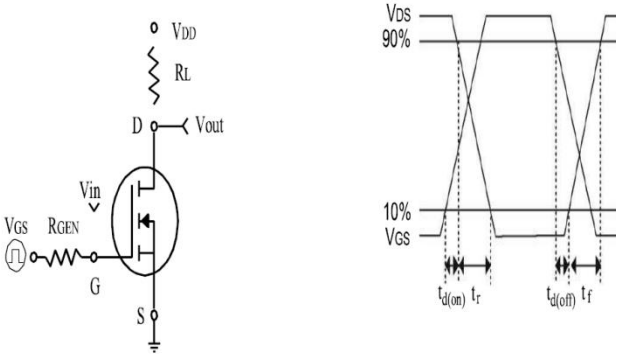
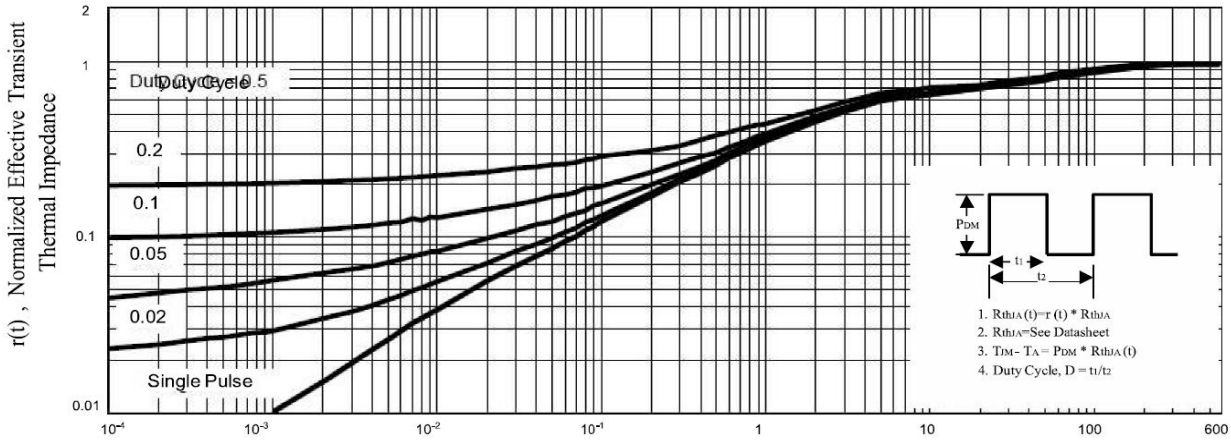


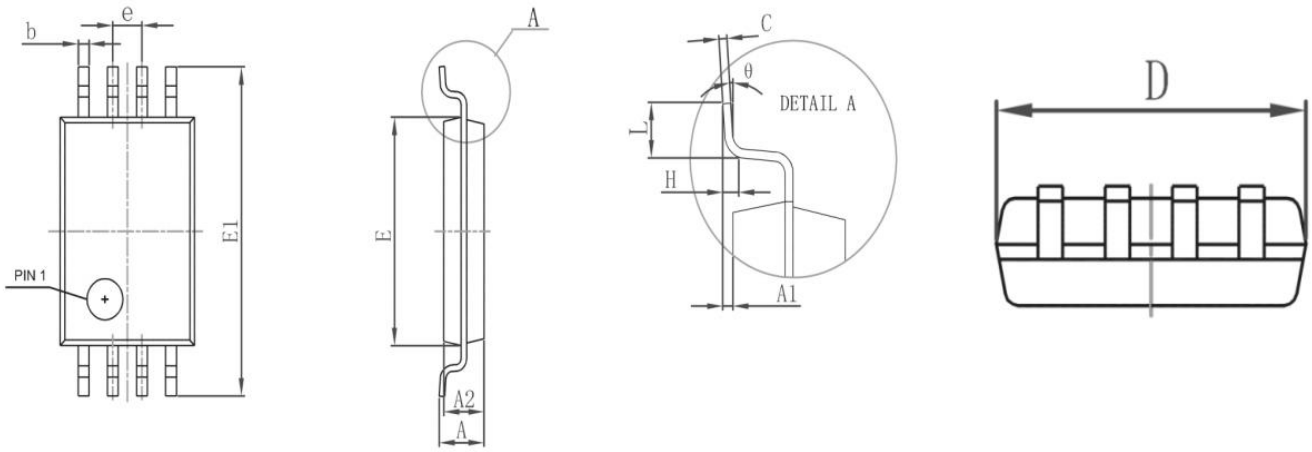
Figure 9. Switching Test Circuit and Switching Waveforms



Square Wave Pulse Duration (sec)

Figure 10. Normalized Thermal Transient Impedance Curve

TSSOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.200	6.600	0.244	0.260
A	-	1.200	-	0.047
A2	0.800	1.050	0.031	0.041
A1	0.000	0.150	0.000	0.006
e	0.650(TYP)		0.260(TYP)	
L	0.450	0.7500	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°