

Features

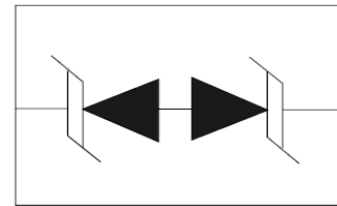
- Ultra-low capacitance: $C_J = 10\text{pF}$ typ
- Stand-off voltage: $\pm 5.5\text{V}$ Max
- Solid-state silicon technology
- Low leakage current
- Low clamping voltage: $V_{CL} = 11.0\text{V}$ typ. @ $I_{PP} = 16\text{A}$ (TLP)
- Compliant to Halogen-free
- Suffix "-Q1" for AEC-Q101



DFN-2L(0402)

Protection Solution to Meet

- IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Surge) 6A (8/20 μs)



Pin Configuration

Mechanical Data

- **Package:** DFN-2L
- **Terminals:** Tin plated lead, solderable per J-STD-002 and JESD22-B102
- **Marking code :** 6A

Maximum Ratings

PARAMETER	SYMBOL	Rating	UNIT
Peak pulse power ($t_p = 8/20\mu\text{s}$)	P_{pk}	72	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	KV
ESD according to IEC61000-4-2 contact discharge		± 30	KV
Junction temperature	T_J	125	$^{\circ}\text{C}$
Operating temperature	T_{OP}	-40~85	$^{\circ}\text{C}$
Storage temperature	T_{STG}	-55~150	$^{\circ}\text{C}$

Electrical Characteristics (T_a=25°C Unless otherwise specified)

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V _{RWM}	V				±5.5
Reverse leakage current	I _R	nA	V _{RWM} = 5.5V			100
Reverse breakdown voltage	V _{BR}	V	I _{BR} = 1mA	6.1	7	
Reverse holding voltage	V _{HOLD}	V	I _{HOLD} = 50mA	6.1	7	
Clamping voltage ¹⁾	V _{CL}	V	I _{PP} = 16A, t _p = 100ns		11.0	
Dynamic resistance ¹⁾	R _{DYN}	Ω			0.28	
Clamping voltage ²⁾	V _{CL}	V	V _{ESD} = 8kV		11.0	
Clamping voltage ³⁾	V _{CL}	V	I _{PP} = 1A, t _p = 8/20μs			8
		V	I _{PP} = 6A, t _p = 8/20μs			12
Junction capacitance	C _J	pF	V _R = 0V, f = 1MHz		10	13
		pF	V _R = 2.5V, f = 1MHz		8	11

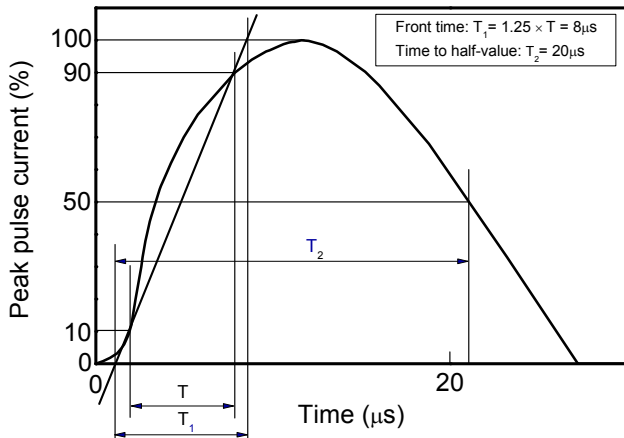
(1). TLP parameter: Z₀ = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

(2). Contact discharge mode, according to IEC61000-4-2.

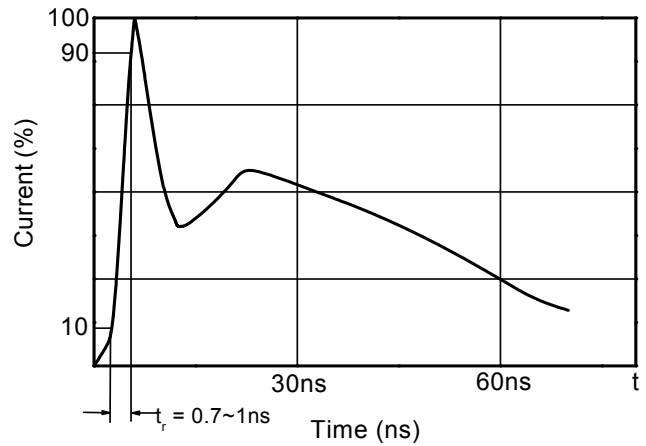
(3). Non-repetitive current pulse, according to IEC61000-4-5.

Typical Characteristics

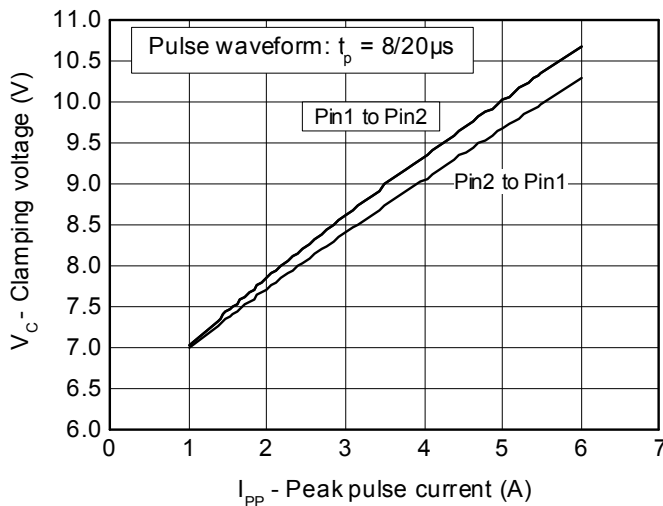
8/20 μ s waveform per IEC61000-4-5



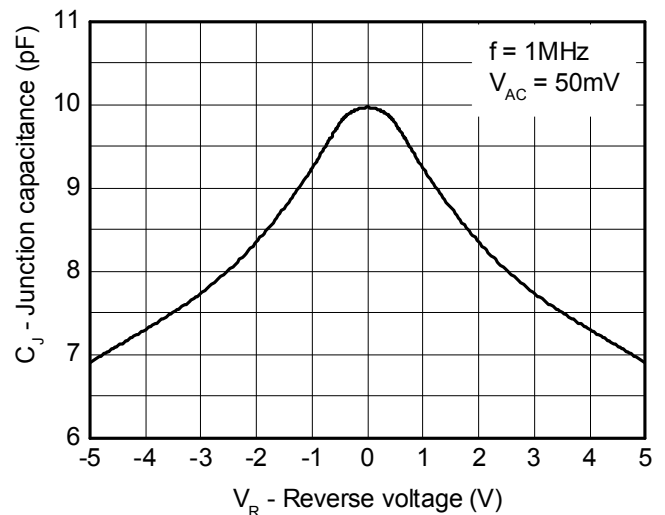
Contact discharge current waveform per IEC61000-4-2



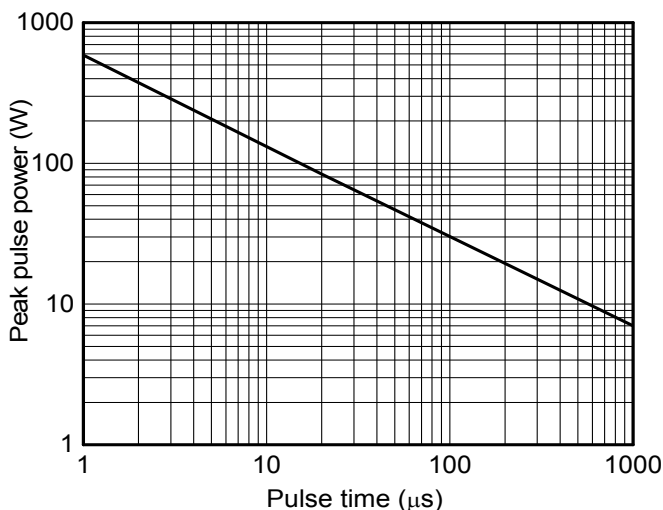
Clamping voltage vs. Peak pulse current



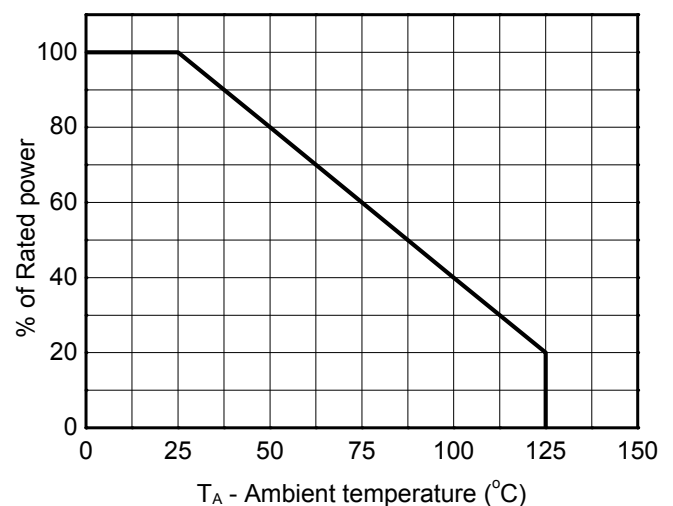
Capacitance vs. Reverse voltage



Non-repetitive peak pulse power vs. Pulse time

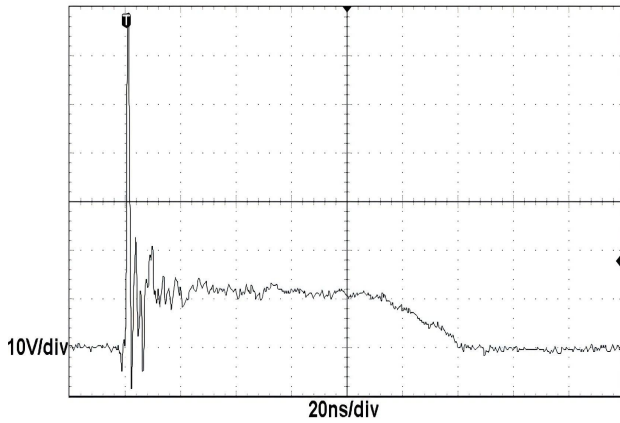


Power derating vs. Ambient temperature

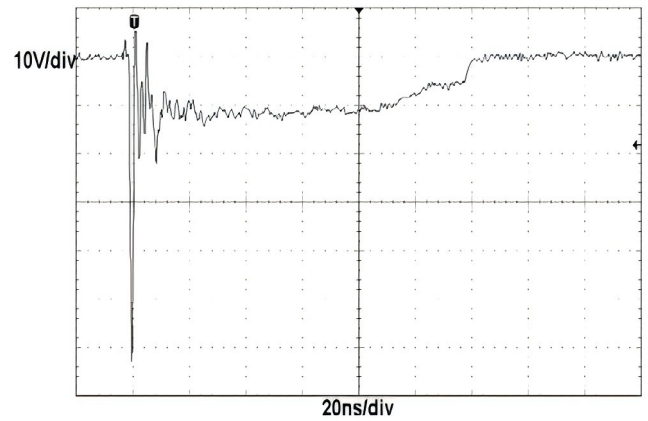


Typical Characteristics

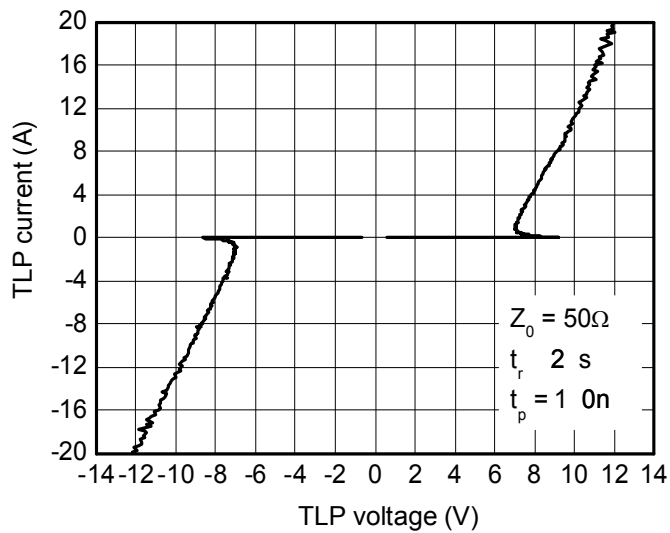
ESD clamping
(+8kV contact discharge per IEC61000-4-2)



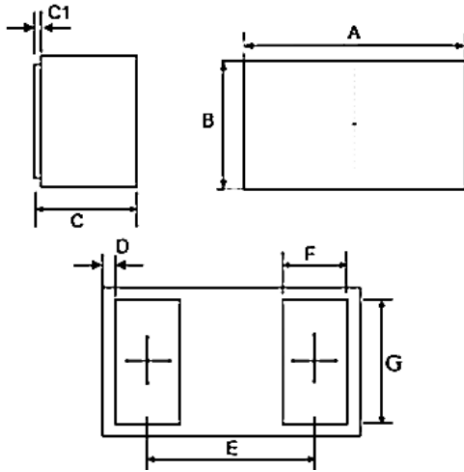
ESD clamping
(-8kV contact discharge per IEC61000-4-2)



TLP Measurement

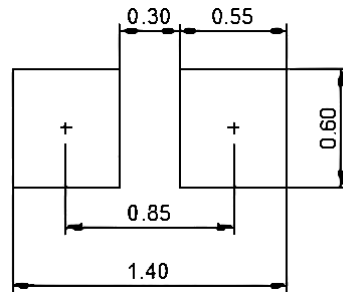


DFN-2L Package Dimensions



Symbol	min. (mm)	Max. (mm)
A	0.95	1.05
B	0.55	0.65
C	0.4	0.5
C1		0.05
D	0.01	0.08
E		0.65
F	0.2	0.3
G	0.45	0.55

Recommend land pattern (Unit:mm)



Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.