AT007SP020MQNH-Q1

P-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-20V	36.5mΩ@-4.5V	-7A
	46.5mΩ@-2.5V	
	60.5mΩ@-1.8V	

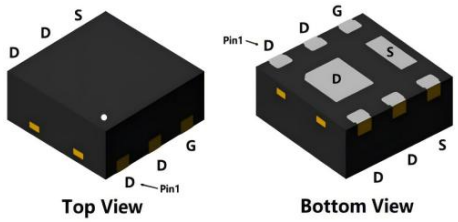
Feature

- Trench power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High speed switching
- Suffix “-Q1” for AEC-Q101

Application

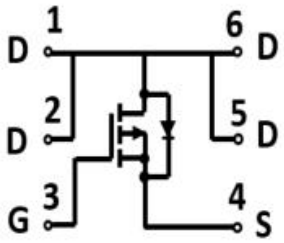
- Battery protection
- Load switch
- Power management

Package



DFN2*2-6L

Circuit diagram



Marking

Absolute maximum ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±10	V
Continuous Drain Current (T_C= 25℃)	I_D	-7	A
Continuous Drain Current (T_C= 70℃)	I_D(70℃)	-5.6	A
Pulsed Drain Current[1)]	I_{DM}	-28	A
Power Dissipation[2)]	P_D	2.2	W
Thermal Resistance Junction to Ambient[3)]	$R_{\theta JA}$	57	℃/ W
Operating Junction Temperature	T_J	-55 ~ +150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} =0V, I_D =-250μA	-20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V, V_{GS} =0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±10V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.62	-1	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-7A		24.5	36.5	mΩ
		V_{GS} =-2.5V, I_D =-5A		33.5	46.5	
		V_{GS} =-1.8V, I_D =-2A		45.5	60.5	
Dynamic characteristics[4)]						
Input Capacitance	C_{iss}	V_{DS} =-10V, V_{GS} =0V, f =1MHz		852		pF
Output Capacitance	C_{oss}			127		
Reverse Transfer Capacitance	C_{rss}			109		
Total Gate Charge	Q_g	V_{DS} =-9V, V_{GS} =-4.5V, I_D =-7A		40.1		nC
Gate-Source Charge	Q_{gs}			8.4		
Gate-Drain Charge	Q_{gd}			8.6		
Turn-on delay time	$t_{d(on)}$	V_{DS} =-9V, V_{GS} =-4.5V, I_D =-1A R_G =2.5Ω		8		nS
Turn-on rise time	t_r			19		
Turn-off delay time	$t_{d(off)}$			75		
Turn-off fall time	t_f			46		
Source-Drain Diode characteristics						
Diode Forward Current	I_S				-7	A
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S =-7A			-1.2	V
Reverse Recovery Time	T_{rr}	I_F =-15A, di/dt =-100A/us		18		nS
Reverse Recovery Charge	Q_{rr}			7.8		nC

Notes:

1) Pulse Test: Pulse Width ≤300us, Duty cycle ≤2%.

2) Pd is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

3) $R_{\theta JA}$ is the sum of the junction to case and case to ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

4) Guaranteed by design, not subject to production.

Typical Characteristics

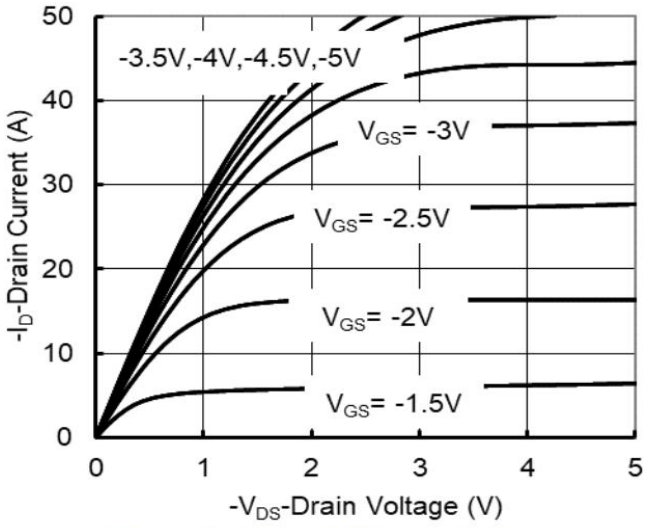


Figure 1. Output Characteristics

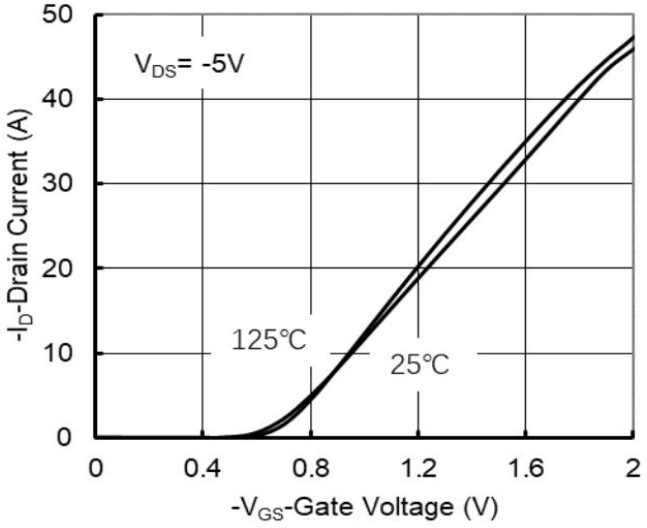


Figure 2. Transfer Characteristics

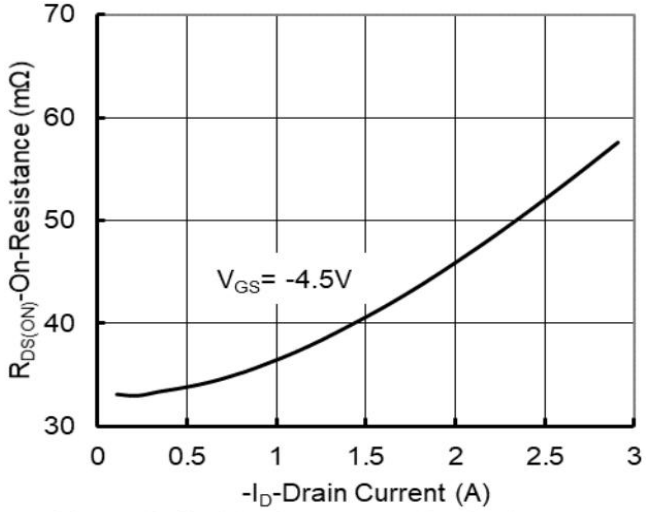


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

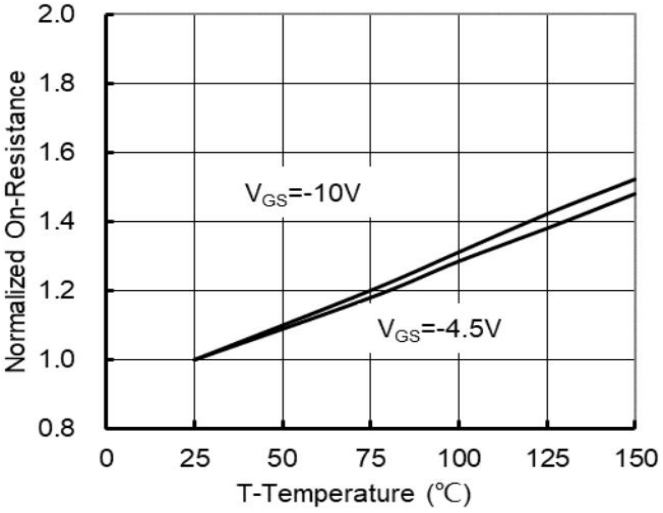


Figure 4. On-Resistance vs. Junction Temperature

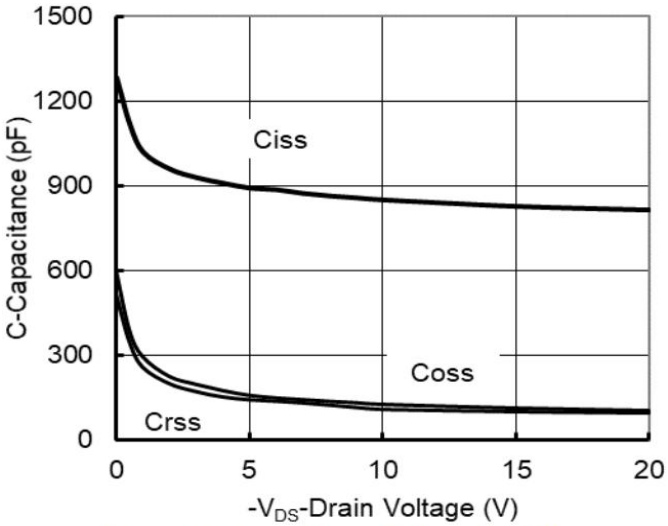


Figure 5. Capacitance Characteristics

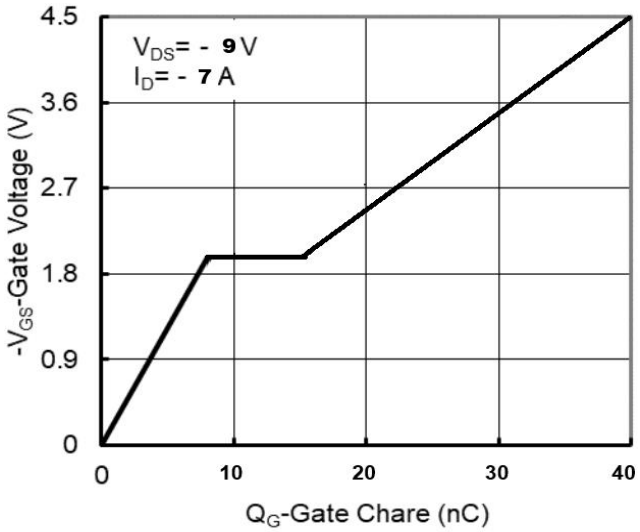


Figure 6. Gate Charge

Typical Characteristics

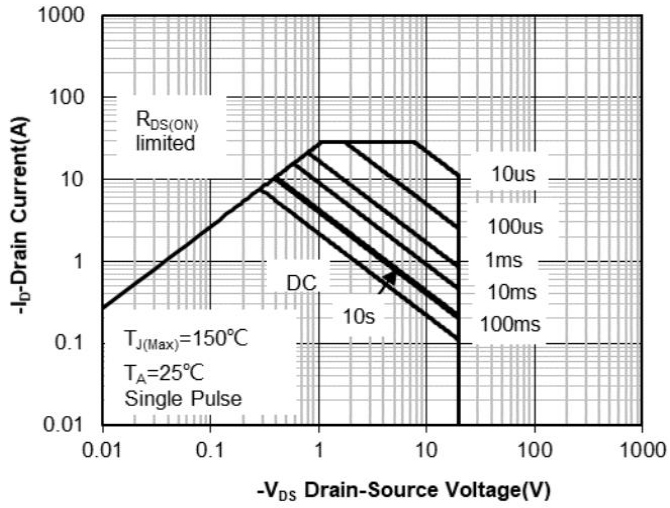


Figure 7. Safe Operation Area

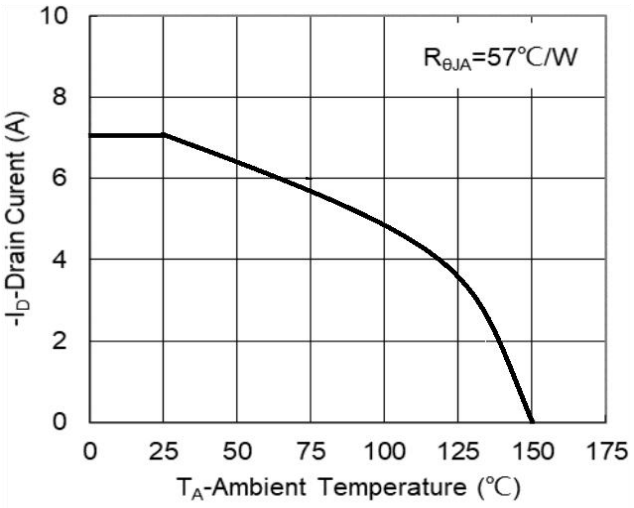


Figure 8. Maximum Continuous Drain Current vs Case Temperature

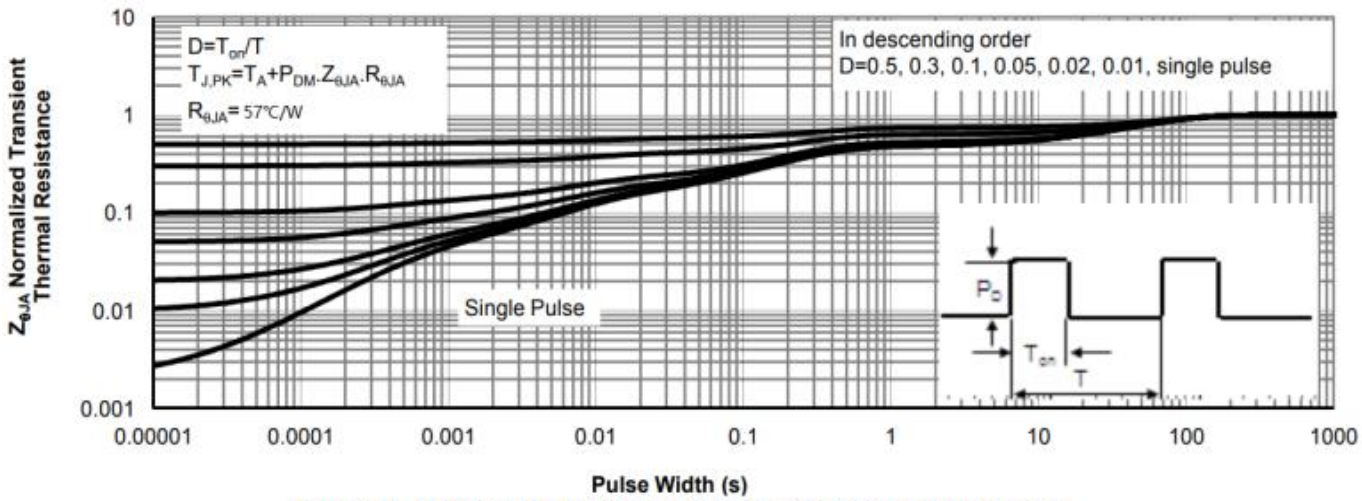
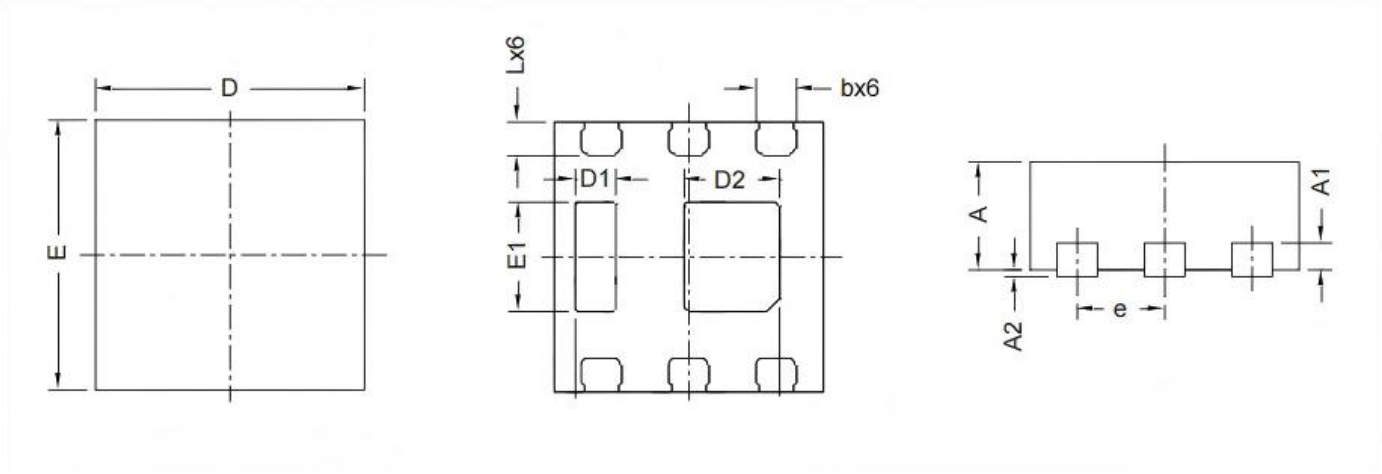


Figure 9. Normalized Maximum Transient Thermal Impedance

DFN2*2-6L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
A	0.350	0.550	0.014	0.022
A1	0.150 BSC.		0.006 BSC.	
A2	-	0.100	-	0.004
D1	0.200	0.400	0.008	0.016
D2	0.610	0.810	0.024	0.032
E1	0.710	0.910	0.028	0.036
L	0.150	0.350	0.006	0.014
b	0.200	0.400	0.008	0.016
e	0.650 BSC.		0.026 BSC.	