AT009DN060MQSP-Q1

N-Channel Enhancement Mode MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
60V	16.8mΩ@10V	9A
	22mΩ@4.5V	

Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses
- Suffix “-Q1” for AEC-Q101

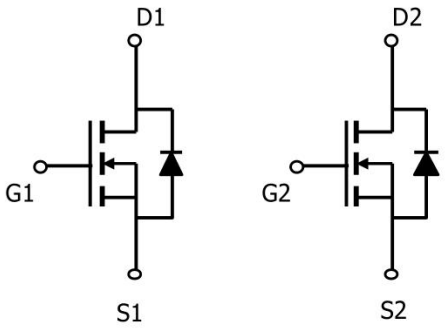
Application

- Load switch
- Power switching application

Package

SOP-8

Circuit diagram



Marking

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Absolute maximum ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	9	A
Continuous Drain Current (T_C=100℃)	I_D(100℃)	7	A
Pulsed Drain Current	I_{DM}	36	A
Power Dissipation	P_D	2.6	W
Thermal Resistance Junction to Ambient[1)]	$R_{\theta JA}$	48	℃/W
Operating Junction Temperature	T_J	-55 ~ +150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_C=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} =0V, I_D =250μA	60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =60V, V_{GS} =0V			1	μA
Gate-body leakage current	I_{GSS}	V_{DS} =0V, V_{GS} =±20V			±100	nA
Gate threshold voltage[2)]	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.2	1.8	2.2	V
Drain-source on-resistance[2)]	$R_{DS(on)}$	V_{GS} =10V, I_D =9A		14.5	16.8	mΩ
		V_{GS} =4.5V, I_D =8A		16	22	
Dynamic characteristics[3)]						
Input Capacitance	C_{iss}	V_{DS} =30V, V_{GS} =0V, f =1MHz		2180		pF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			270		
Total Gate Charge	Q_g	V_{DS} =30V, V_{GS} =10V, I_D =9A		58		nC
Gate-Source Charge	Q_{gs}			8		
Gate-Drain Charge	Q_{gd}			17		
Turn-on delay time	$t_{d(on)}$	V_{DS} =30V, V_{GS} =10V, R_L =1Ω R_G =3Ω		8.5		nS
Turn-on rise time	t_r			6		
Turn-off delay time	$t_{d(off)}$			30		
Turn-off fall time	t_f			5		
Source-Drain Diode characteristics						
Diode Forward Current	I_S				9	A
Diode Forward voltage	V_{SD}	V_{GS} =0V, I_S =9A			1.2	V
Reverse recover time	T_{rr}	I_F =9A, di/dt =100A/us[2)] T_J=25℃		30		nS
Reverse recovery charge	Q_{rr}			44		nC

Notes:

1) Surface Mounted on FR4 Board, t ≤10 sec.

2) Pulse Test: Pulse Width ≤300μs, Duty Cycle ≤2%.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

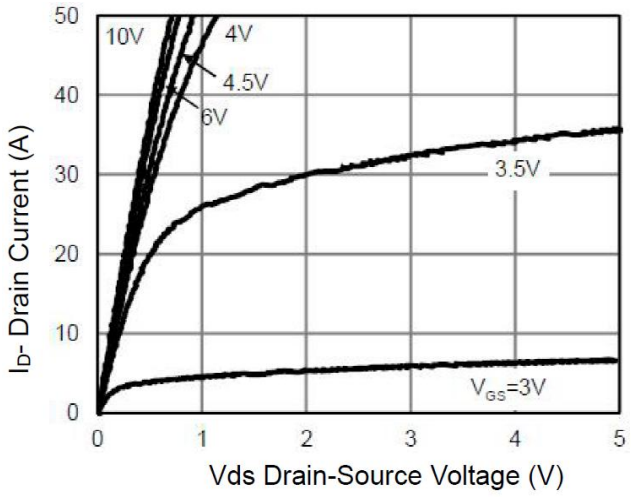


Figure 1 Output Characteristics

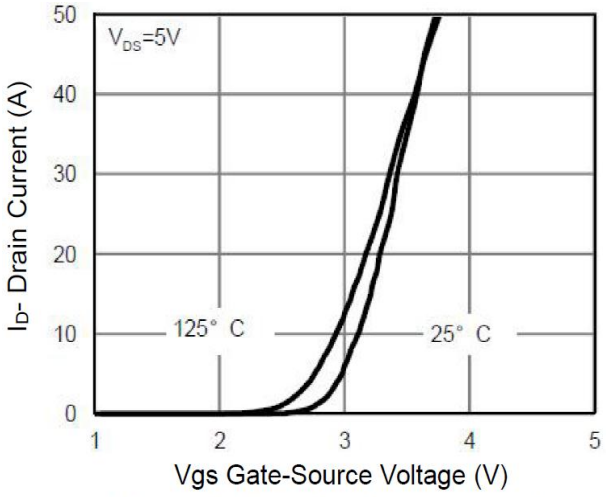


Figure 2 Transfer Characteristics

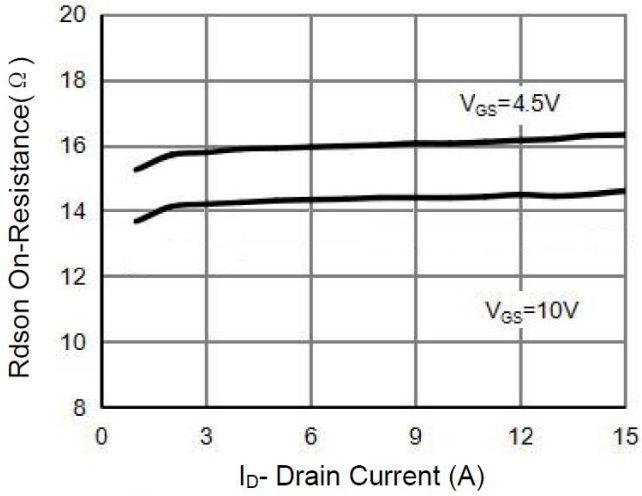


Figure 3 Rdson- Drain Current

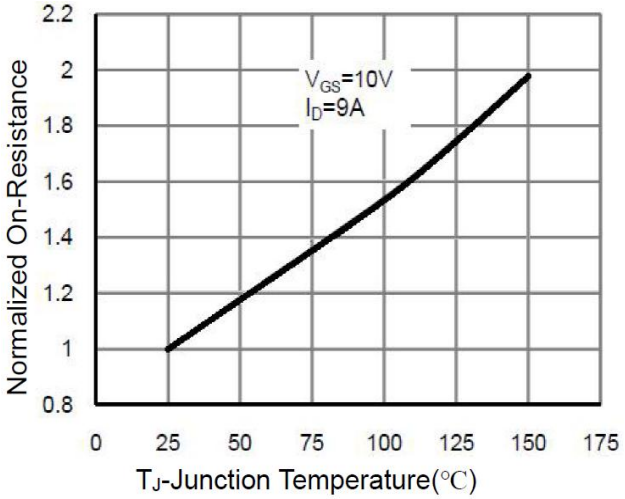


Figure 4 Rdson-JunctionTemperature

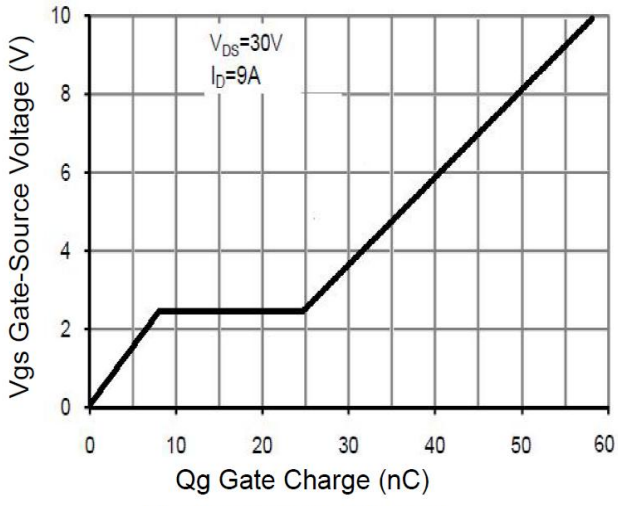


Figure 5 Gate Charge

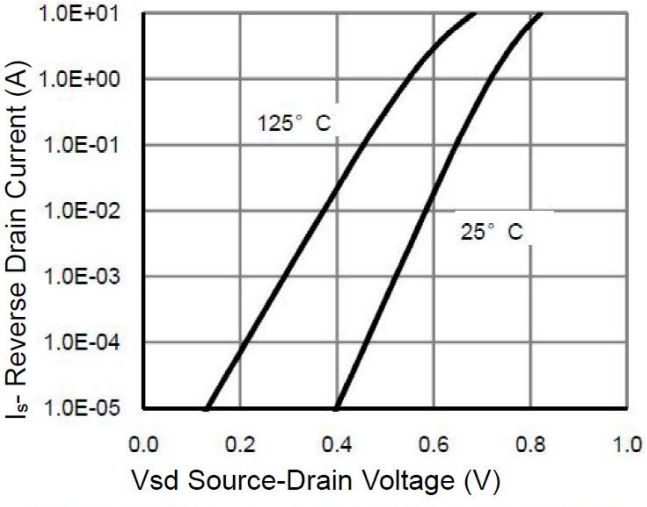


Figure 6 Source- Drain Diode Forward

Typical Characteristics

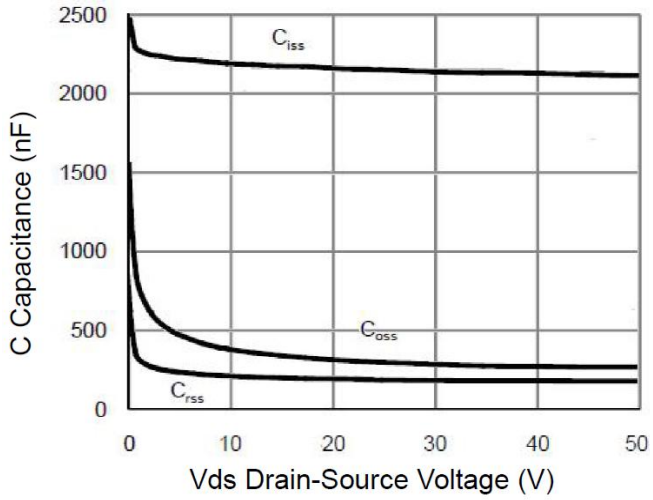


Figure 7 Capacitance vs Vds

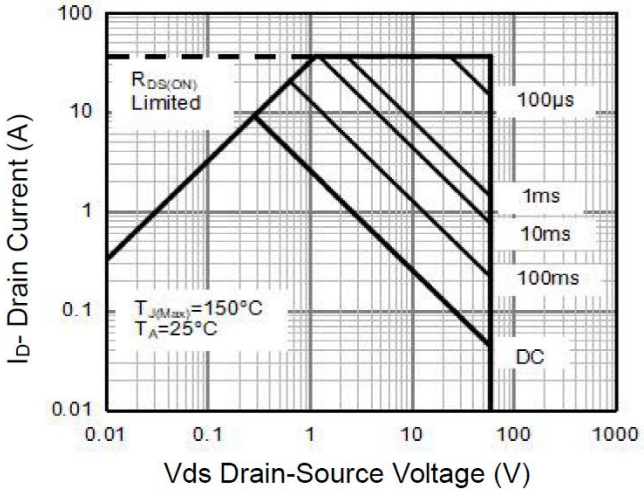


Figure 8 Safe Operation Area

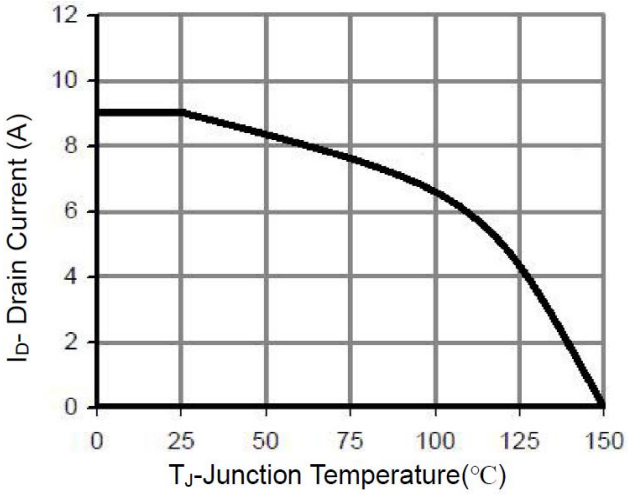


Figure 9 Current De-rating

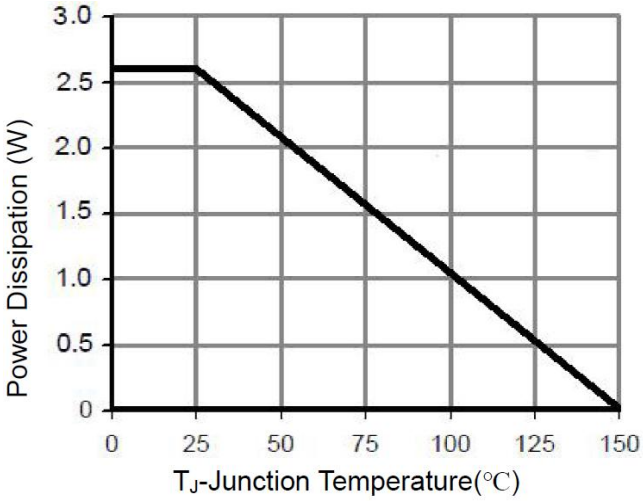


Figure 10 Power De-rating

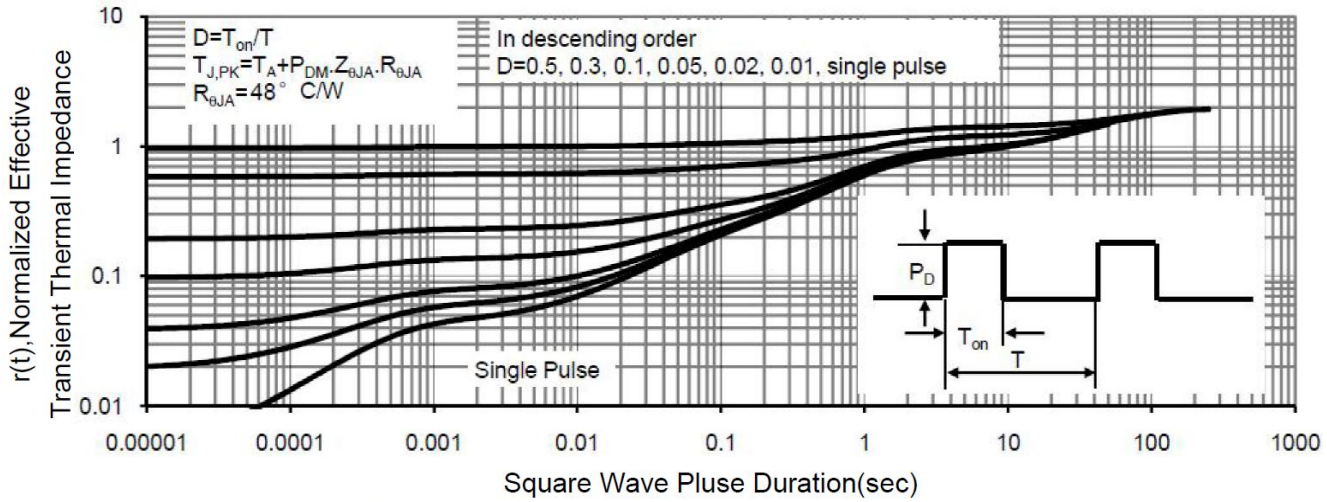
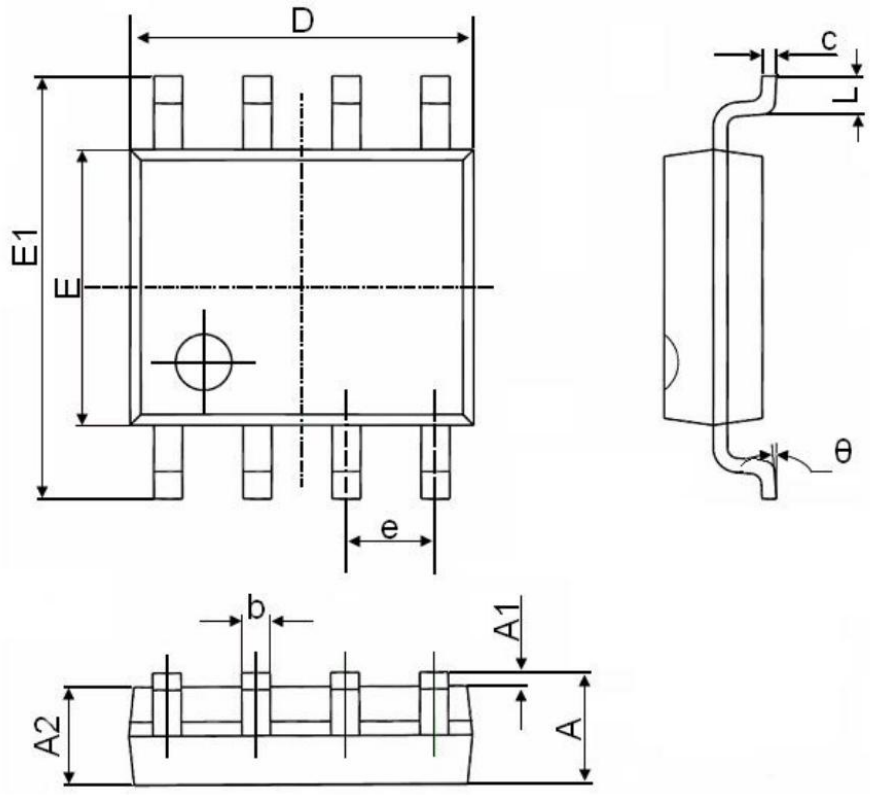


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC.		0.050 BSC.	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°