

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-20V	19mΩ@-4.5V	-30A
	22mΩ@-2.5V	
	30mΩ@-1.8V	

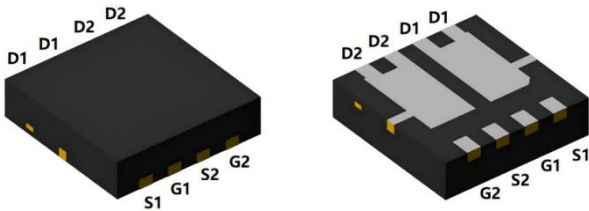
Feature

- Trench power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High speed switching
- Suffix“-Q1”for AEC-Q101

Application

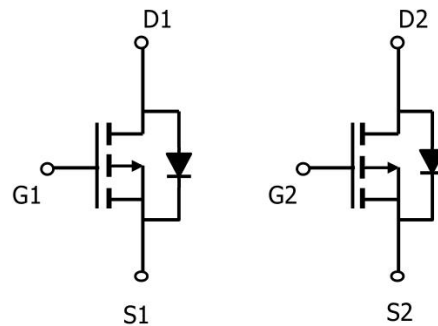
- Power management
- Battery protection
- Load switch

Package

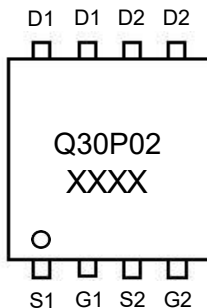


DFN3.3*3.3-8L

Circuit diagram



Marking



Absolute maximum ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current ($T_C=25^\circ\text{C}$)	I_D	-30	A
Continuous Drain Current ($T_A=25^\circ\text{C}$)		-10	A
Pulsed Drain Current ¹⁾	I_{DM}	-55	A
Single Pulse Avalanche Energy	E_{AS}	31	mJ
Power Dissipation ²⁾ ($T_C=25^\circ\text{C}$)	P_D	21	W
Thermal Resistance Junction to Case	$R_{\theta JC}$	5.9	$^\circ\text{C}/\text{W}$
Operating Junction Temperature	T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Electrical characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-20\text{V}, V_{GS}=0\text{V}$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 10\text{V}$			± 100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-0.4	-0.62	-1	V
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=-4.5\text{V}, I_D=-15\text{A}$		11	19	m Ω
		$V_{GS}=-2.5\text{V}, I_D=-8\text{A}$		14	22	
		$V_{GS}=-1.8\text{V}, I_D=-6\text{A}$		20	30	
Dynamic characteristics³⁾						
Input Capacitance	C_{iss}	$V_{DS}=-10\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		2992		pF
Output Capacitance	C_{oss}		330			
Reverse Transfer Capacitance	C_{rss}		272			
Total Gate Charge	Q_g	$V_{DS}=-15\text{V}, V_{GS}=-10\text{V}$ $I_D=-9.1\text{A}$		72.8		nC
Gate-Source Charge	Q_{gs}		6.6			
Gate-Drain Charge	Q_{gd}		10.1			
Turn-on delay time	$t_{d(on)}$	$V_{DS}=-15\text{V}, V_{GS}=-10\text{V}$ $I_D=-6\text{A}, R_G=2.5\Omega$		7		nS
Turn-on rise time	t_r		33			
Turn-off delay time	$t_{d(off)}$		130			
Turn-off fall time	t_f		132			
Source-Drain Diode characteristics						
Diode Forward Current	I_S				-30	A
Diode Forward voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=-30\text{A}$			-1.2	V
Reverse Recovery Time	T_{rr}	$I_F=-6\text{A}, di/dt=-100\text{A}/\mu\text{s}$		67		nS
Reverse Recovery Charge	Q_{rr}		34		nC	

Notes:

1) Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2) P_D is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

3) Guaranteed by design, not subject to production testing.

Typical Characteristics

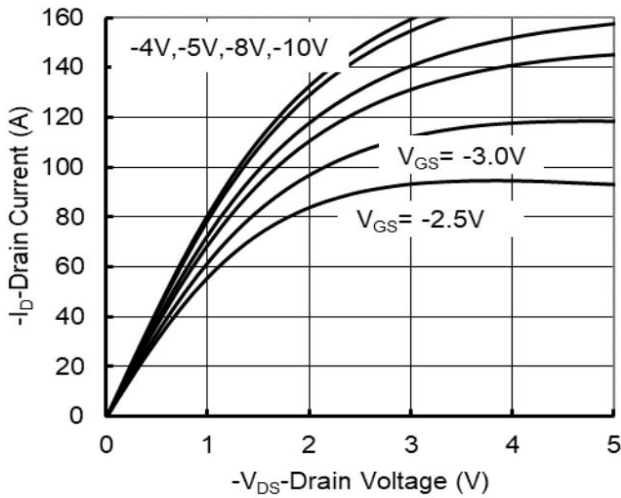


Figure 1. Output Characteristics

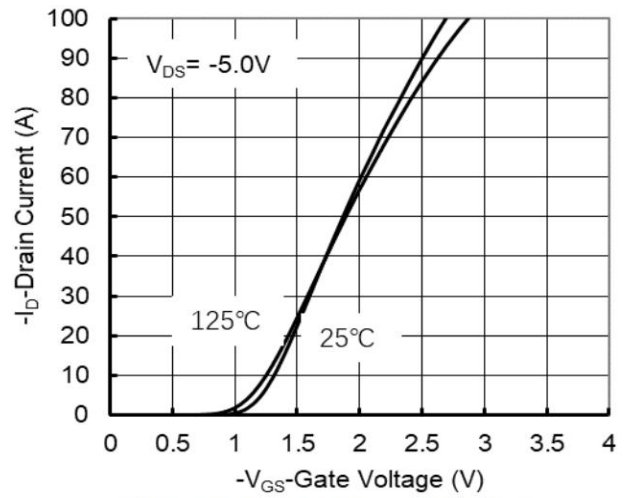


Figure 2. Transfer Characteristics

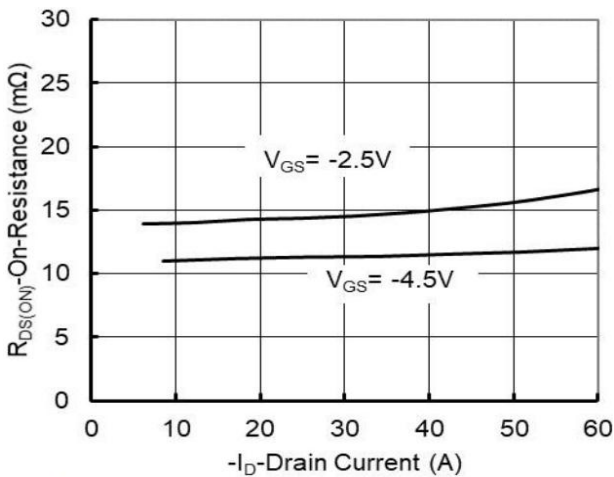


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

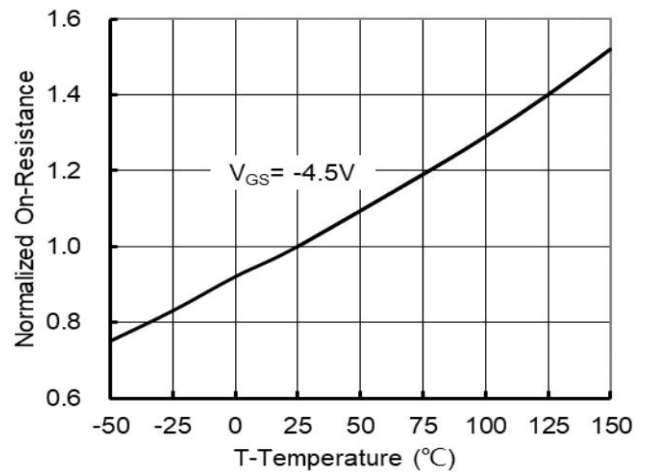


Figure 4. On-Resistance vs. Junction Temperature

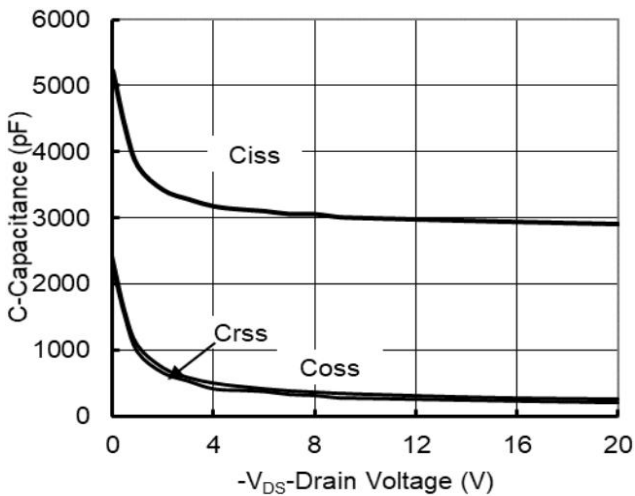


Figure 5. Capacitance Characteristics

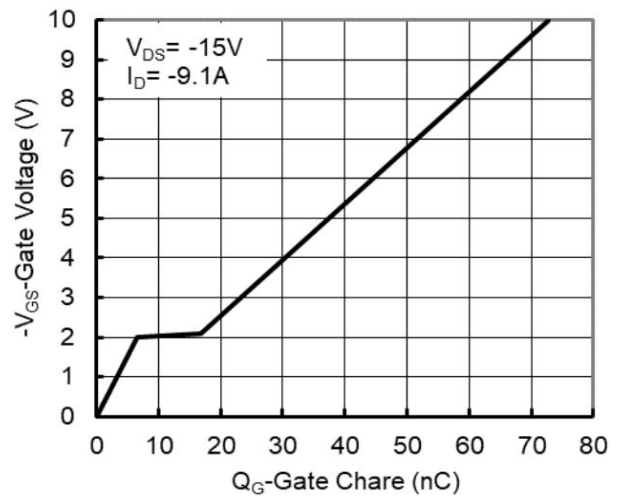


Figure 6. Gate Charge

Typical Characteristics

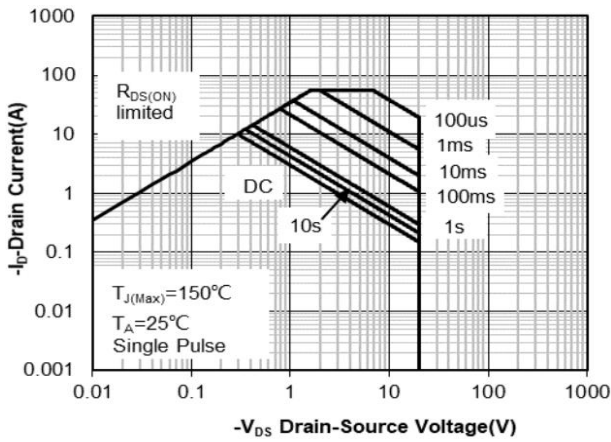


Figure 7. Safe Operation Area

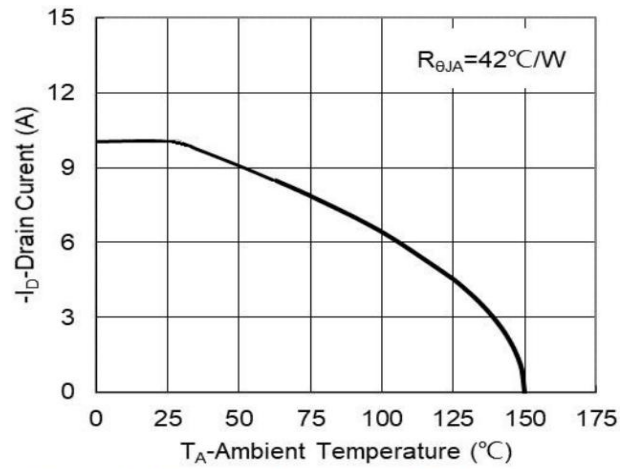


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

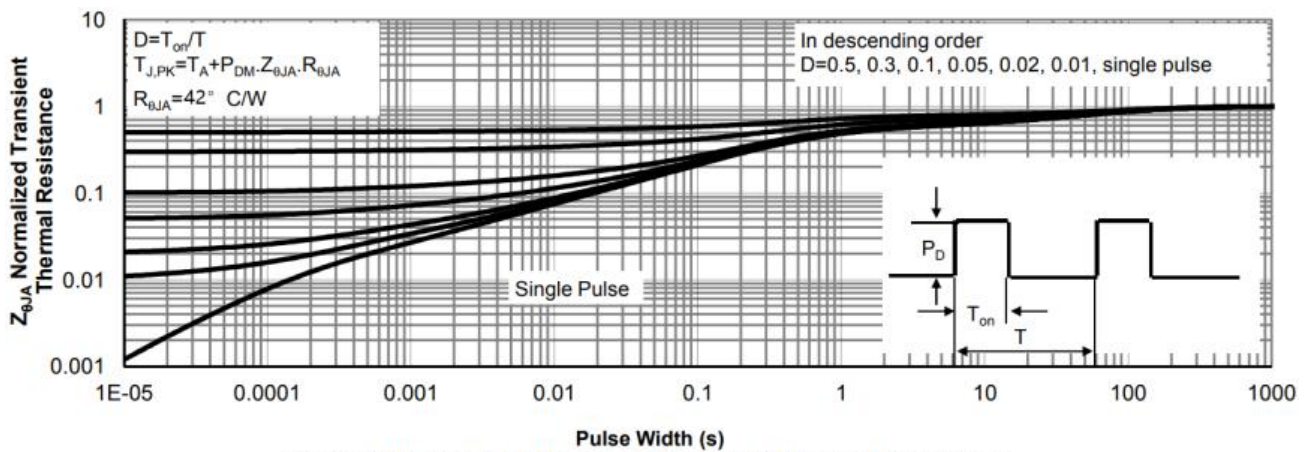
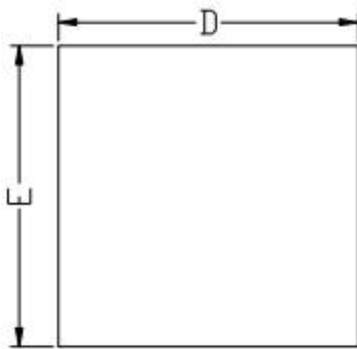
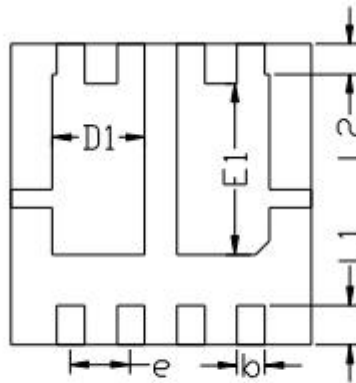


Figure 9. Normalized Maximum Transient Thermal Impedance

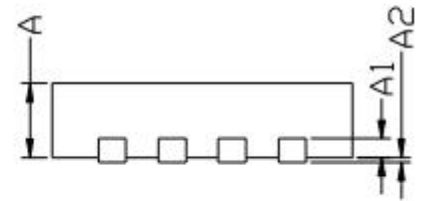
DFN3.3*3.3-8L Package Information



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	3.150	3.350	0.124	0.132
E	3.150	3.350	0.124	0.132
A	0.700	0.900	0.028	0.035
A1	0.200 BSC.		0.008 BSC.	
A2	0.000	0.100	0.000	0.004
D1	0.900	1.100	0.035	0.043
E1	1.750	1.950	0.069	0.077
L1	0.325	0.525	0.013	0.021
L2	0.325 BSC.		0.013 BSC.	
b	0.200	0.400	0.008	0.016
e	0.650 BSC.		0.026 BSC.	