AT50P06S-Q1

P-Channel Enhancement Mode Power MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	I_D
-60V	28mΩ@10V	-50A

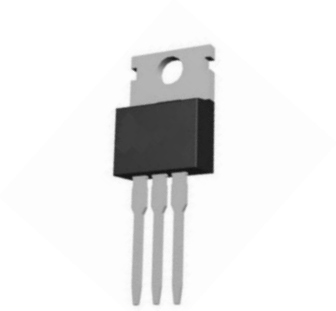
Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Suffix "-Q1" for AEC-Q101

Application

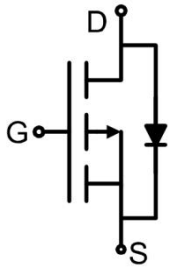
- Load switch

Package



TO-220AB

Circuit diagram



Marking

AT50P06S-Q1

P-Channel Enhancement Mode Power MOSFET

Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	-50	A
Pulsed Drain Current	I_{DM}	-150	A
Power Dissipation	P_D	95	W
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.31	℃/W
Single pulse avalanche energy	E_{AS}	722	mJ
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55 ~ +150	℃

Electrical characteristics (T_A=25 °C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-60			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-60V,V_{GS} = 0V			-1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V			±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-2.0		-3.5	V
Drain-source on-resistance[1)]	$R_{DS(on)}$	V_{GS} =-10V, I_D =-20A		23	28	mΩ
Forward transconductance[1)]	g_{FS}	V_{DS} =-10V, I_D =-20A		25		S
Dynamic characteristics[2)]						
Input Capacitance	C_{iss}	V_{DS} =-25V,V_{GS} =0V,f =1MHz		6460		pF
Output Capacitance	C_{oss}			719		
Reverse Transfer Capacitance	C_{rss}			535		
Total Gate Charge	Q_g	V_{DS} =-30V,V_{GS} =-10V, ID =-20A		75		nC
Gate-Source Charge	Q_{gs}			16		
Gate-Drain Charge	Q_{gd}			19		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-30V,V_{GS}=-10V, R_L=1.5Ω,R_{GEN}=3Ω		15		nS
Turn-on rise time	t_r			17		
Turn-off delay time	$t_{d(off)}$			40		
Turn-off fall time	t_f			45		
Source-Drain Diode characteristics						
Diode Forward Current[1)]	I_S				-20	A
Diode Forward voltage	V_{DS}	V_{GS} =0V, I_S=-20A			-1.2	V
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =-20A di/dt = 100A/μs [1)]		50		nS
Reverse Recovery Charge	Q_{rr}			59		nC

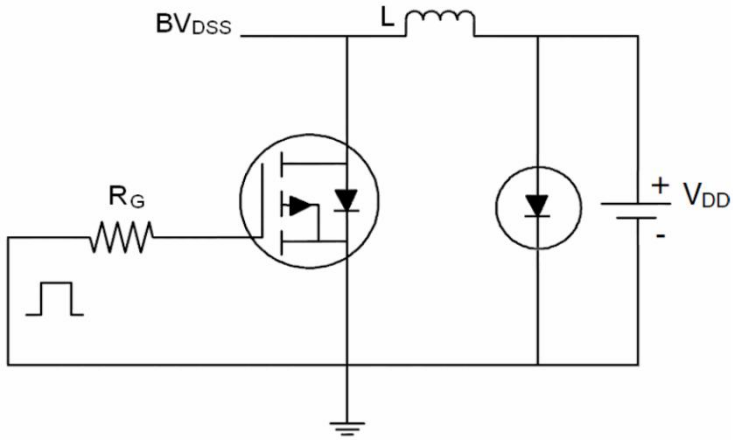
Notes:

1) Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.

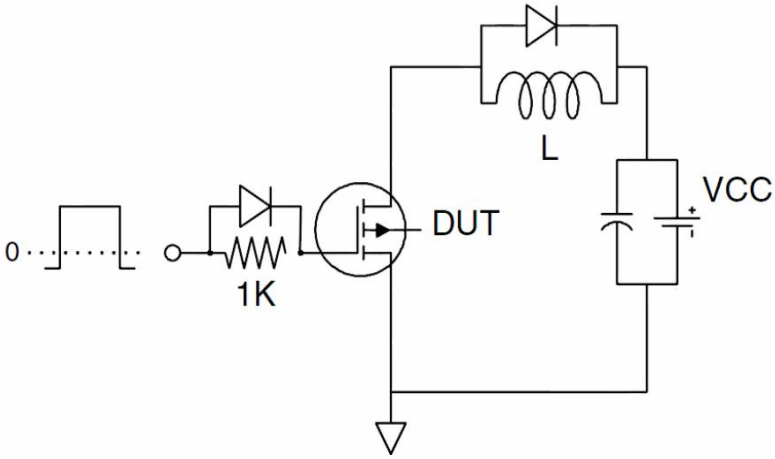
2) Guaranteed by design, not subject to production testing.

Test Circuit

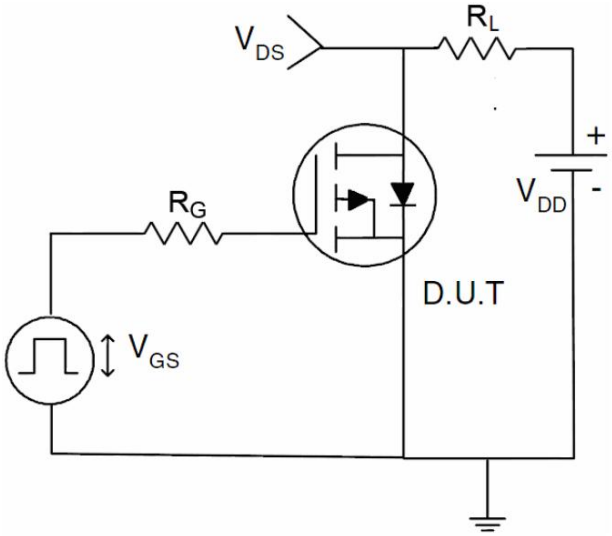
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



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Typical Characteristics

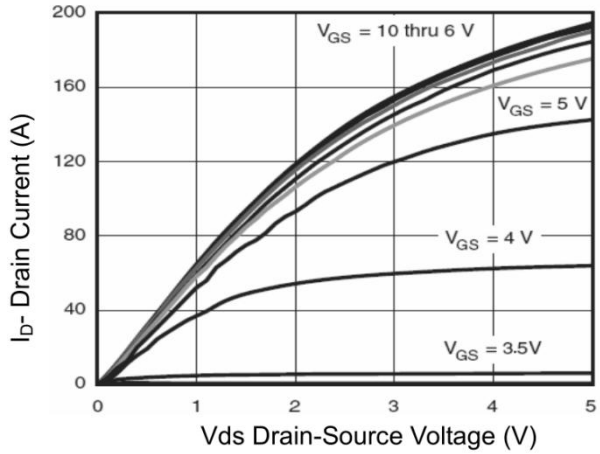


Figure 1 Output Characteristics

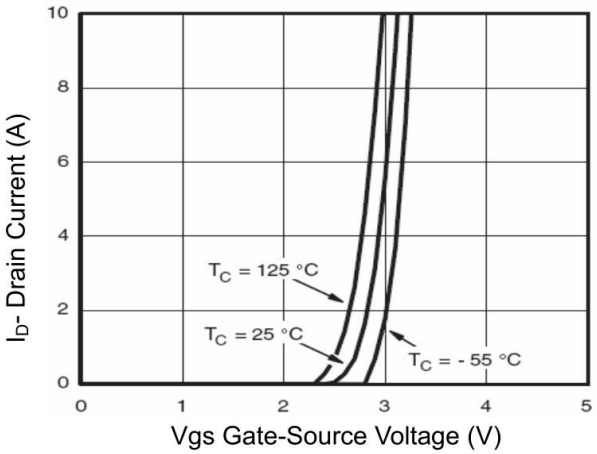


Figure 2 Transfer Characteristics

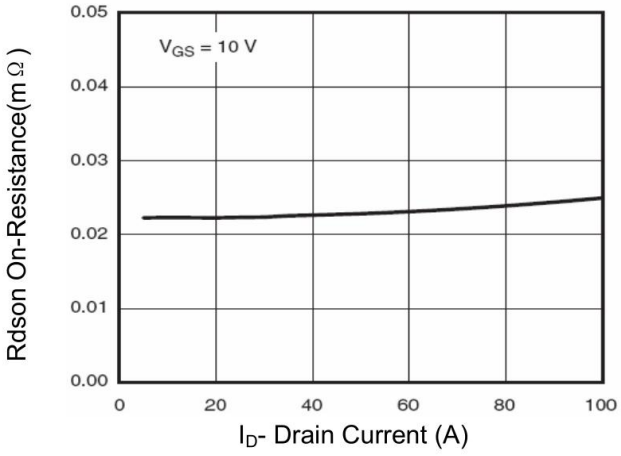


Figure 3 Rdson- Drain Current

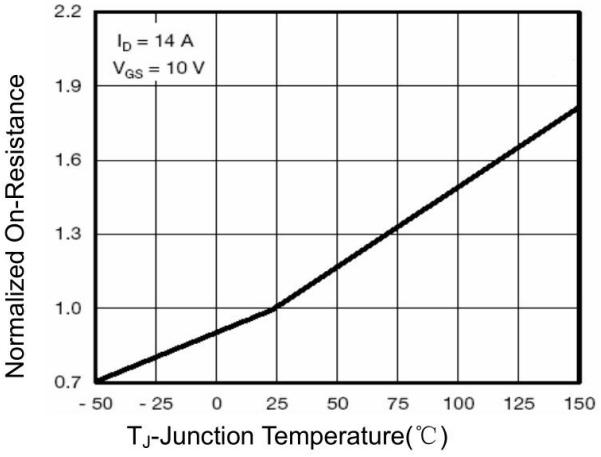


Figure 4 Rdson-Junction Temperature

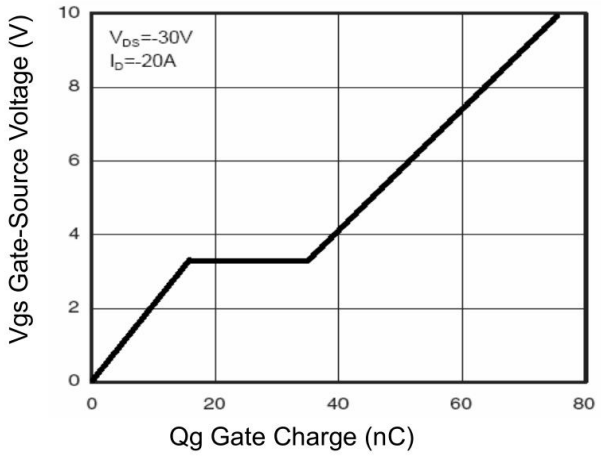


Figure 5 Gate Charge

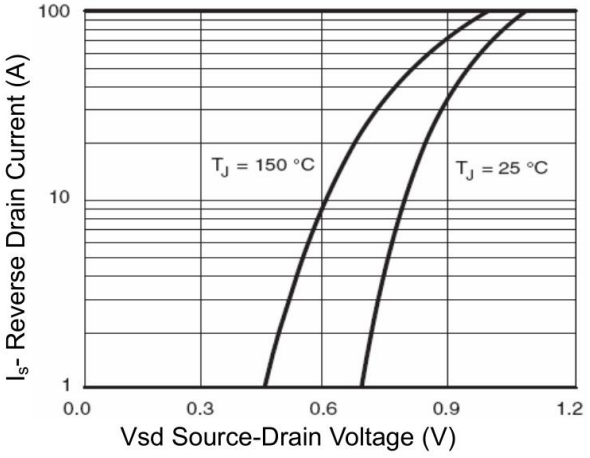


Figure 6 Source- Drain Diode Forward

Typical Characteristics

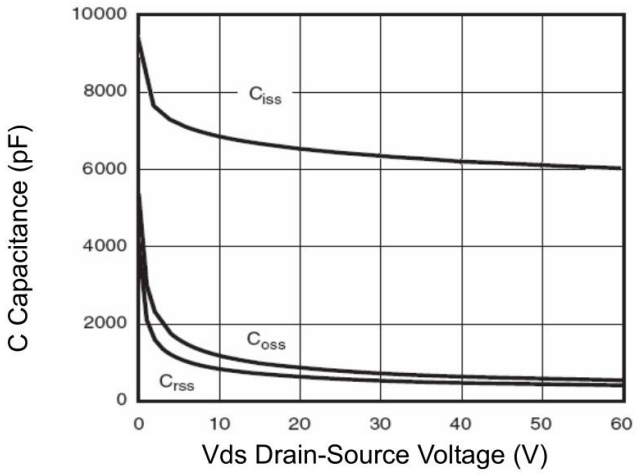


Figure 7 Capacitance vs Vds

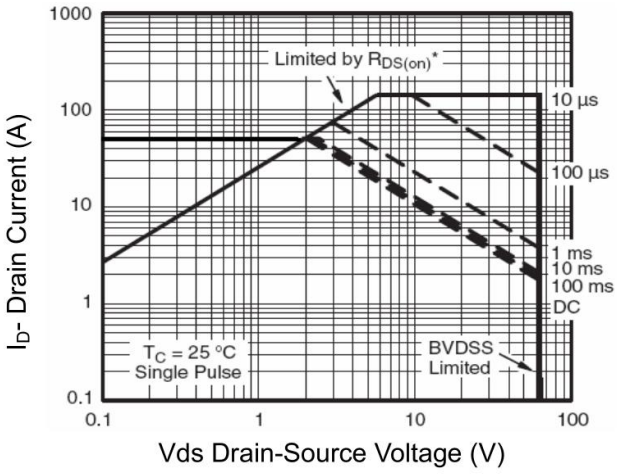


Figure 8 Safe Operation Area

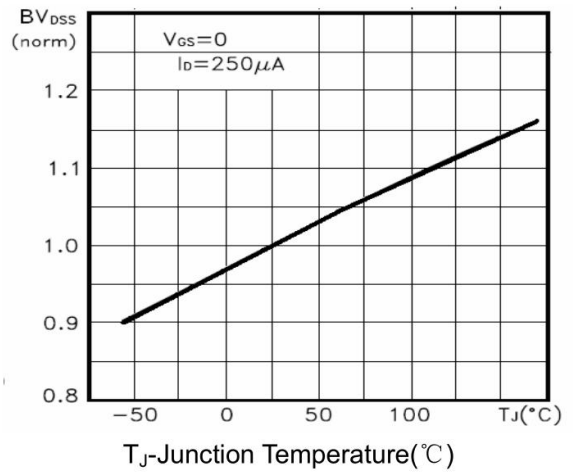


Figure 9 BV_{DSS} vs Junction Temperature

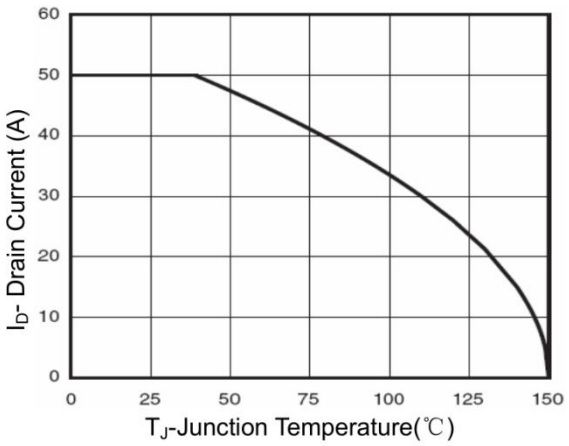


Figure 10 ID Current Derating vs Junction Temperature

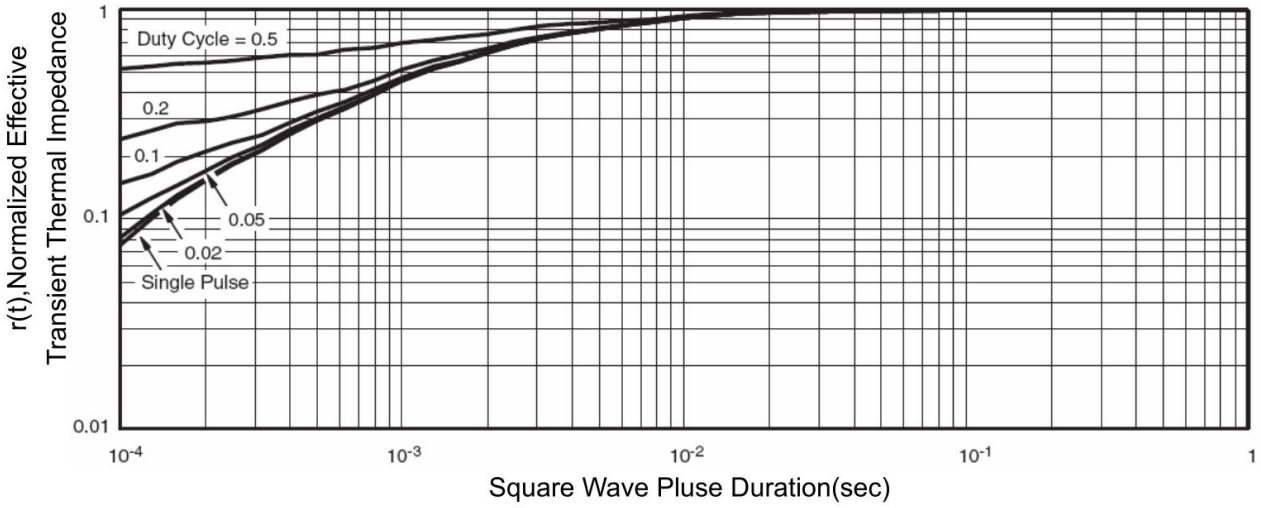
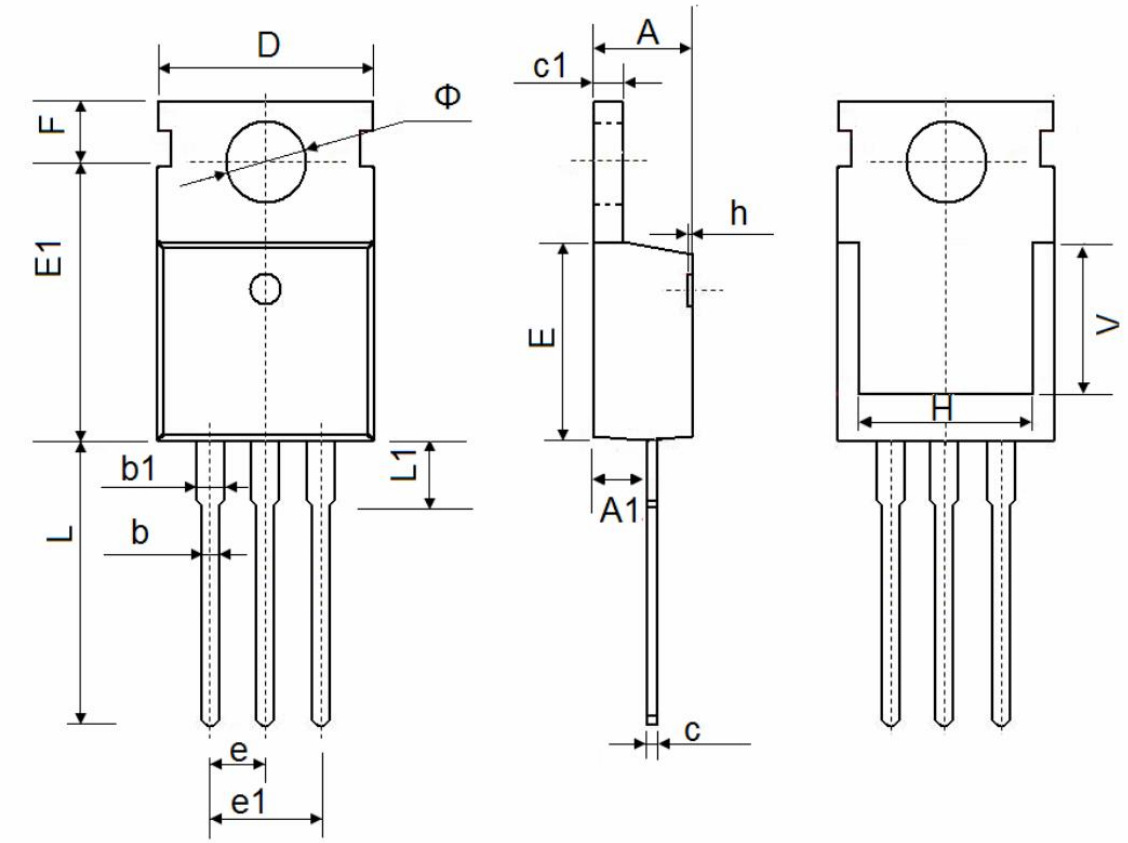


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220AB Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150