

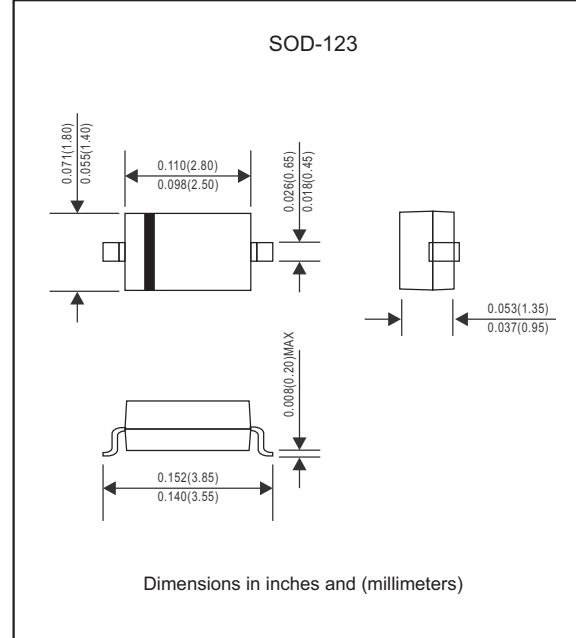
Features

- Batch process design, excellent power dissipation offers better reverse leakage current and thermal resistance.
- Low profile surface mounted application in order to optimize board space.
- Low power loss, high efficiency.
- High current capability, low forward voltage drop.
- High surge capability.
- Guardring for overvoltage protection.
- Very tiny plastic SMD package.
- Ultra high-speed switching.
- Silicon epitaxial planar chip, metal silicon junction.
- Lead-free parts meet environmental standards of MIL-STD-19500 /228
- Compliant to Halogen-free
- Suffix "-Q1" for AEC-Q101

Mechanical data

- Epoxy:UL94-VO rated flame retardant
- Case : Molded plastic, SOD-123
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity : Indicated by cathode band
- Mounting Position : Any

Package outline



Maximum ratings and Electrical Characteristics (AT $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	Symbol	MIN.	TYP.	MAX.	UNIT
Forward rectified current	See Fig.1	I_O			1.0	A
Forward surge current	8.3ms single half sine-wave (JEDEC methode)	I_{FSM}			9	A
Reverse current	$V_R = V_{RRM} \quad T_J = 25^\circ\text{C}$ $V_R = V_{RRM} \quad T_J = 100^\circ\text{C}$	I_R			1.0 10	mA
Thermal resistance	Junction to ambient	$R_{\theta JA}$		200		$^\circ\text{C}/\text{W}$
Diode junction capacitance	f=1MHz and applied 4V DC reverse voltage	C_J		120		pF
Storage temperature		T_{STG}	-55		+150	$^\circ\text{C}$

SYMBOLS	V_{RRM}^{*1} (V)	V_{RMS}^{*2} (V)	V_R^{*3} (V)	V_F^{*4} (V)	Operating temperature $T_J, (^\circ\text{C})$
B5819W-Q1	40	28	40	0.60	-55 to +125

*1 Repetitive peak reverse voltage

*2 RMS voltage

*3 Continuous reverse voltage

*4 Maximum forward voltage@ $I_F=1.0\text{A}$

Rating and characteristic curves (B5819W-Q1)

FIG.1-TYPICAL FORWARD CURRENT DERATING CURVE

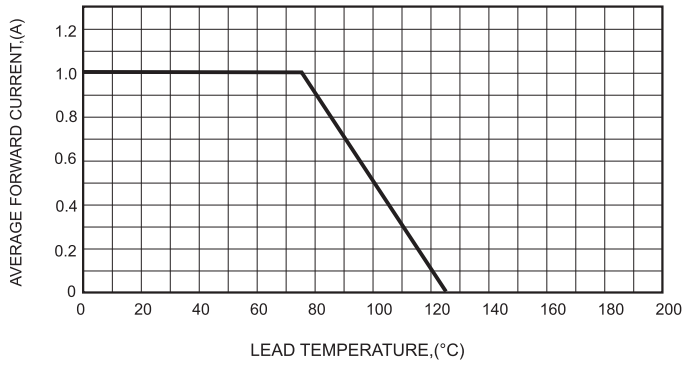


FIG.2-TYPICAL FORWARD CHARACTERISTICS

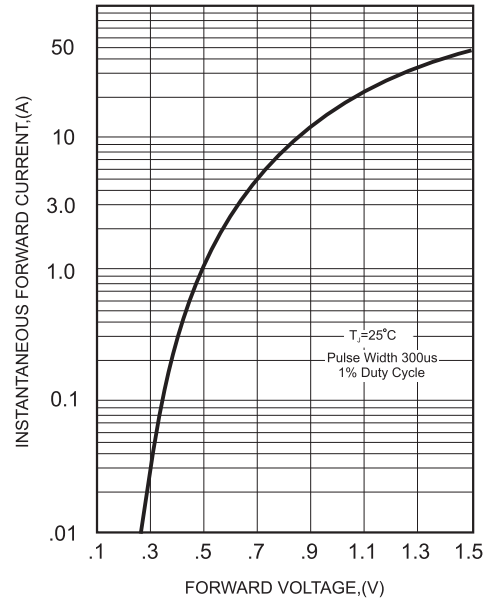


FIG.3-MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT

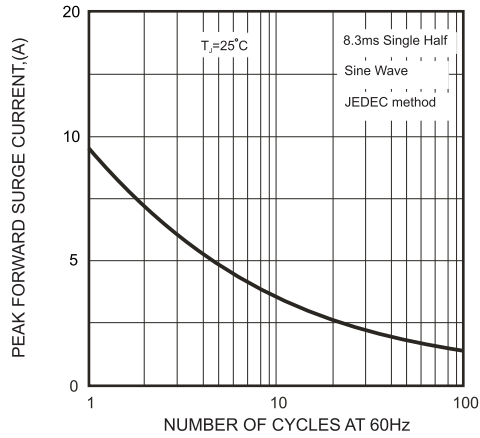


FIG.5 - TYPICAL REVERSE CHARACTERISTICS

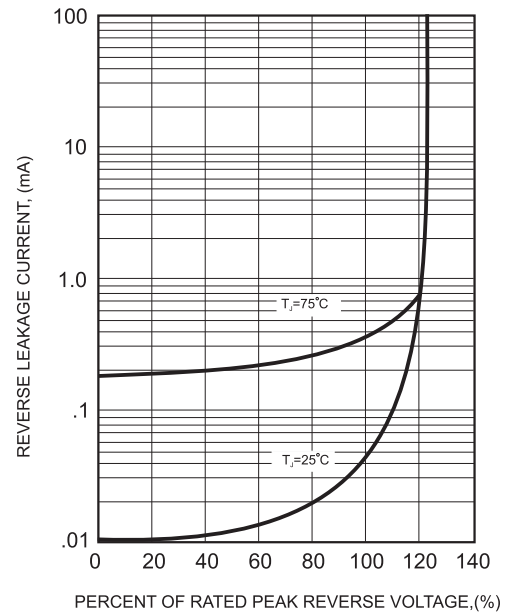
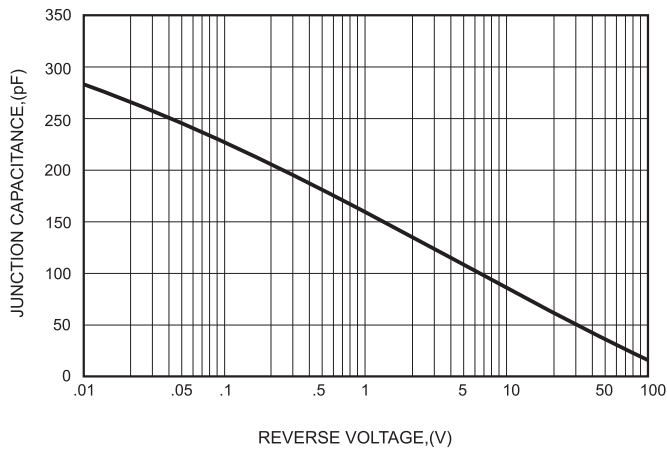
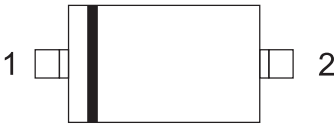



FIG.4-TYPICAL JUNCTION CAPACITANCE



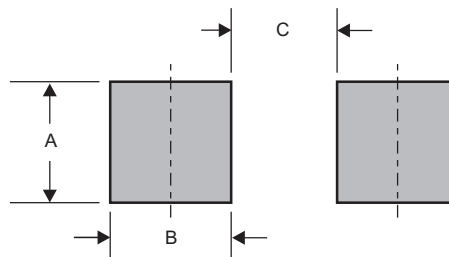
Pinning information

Pin	Simplified outline	Symbol
Pin1 cathode Pin2 anode		

Marking

Type number	Marking code
B5819W-Q1	SL

Suggested solder pad layout



Dimensions in inches and (millimeters)

PACKAGE	A	B	C
SOD-123	0.048 (1.22)	0.036 (0.91)	0.093 (2.36)