LDP5S24CA THRU LDP5S85CA

5000W Surface Mount Transient Voltage Suppressors-24V-85V

Features

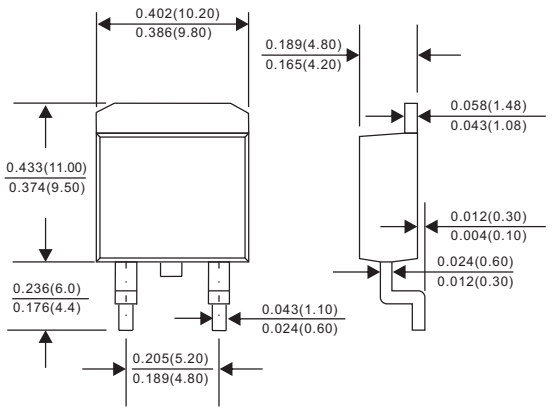
- For surface mounted applications
- Low-profile package
- Ideal for automated placement
- Low incremental surge resistance, excellent clamping capability
- Compliant to Halogen-free

Mechanical Data

- Package: TO-263AB/D2PAK
- Molding compound meets UL 94 V-0 flammability rating,RoHS-compliant
- Terminals: Matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Package outline

TO-263AB/D2PAK



Dimensions in inches and (millimeters)

Absolute Maximum Ratings (Ta = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Peak pulse power dissipation with 10/1000us waveform (1)(2) (fig.1)		P_{PPM}	5000	W
Power dissipation on infinite heatsink at T_L = 75℃		P_D	6.5	W
Peak pulse current with 10/1000us waveform (1)		I_{PPM}	See next table	A
Electrostatic Discharge	IEC61000-4-2 air discharge	ESD	±30	kV
	IEC61000-4-2 contact discharge		±30	kV
Thermal resistance Junction to case (3)		Rth_{JC}	0.24	℃/W
Operating junction temperature range		T_{STG}	-65 to +175	℃
Operating junction and storge temperature range		T_J	-55 to +175	℃

Notes:
(1) Non-repetitive current pulse, per Fig. 3 and derated above T_A = 25℃ per Fig.2.
(2) Mounted on 0.6 x 0.6" (16.0 x 16.0 mm) copper pads to each terminal
(3) Mounted on minimum recommended pad layout

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Electrical Characteristics (T=25°C, RH=45%-75%, unless otherwise noted)

Device Type	Reverse Stand-off Voltage	Breakdown Voltage VBR @ IT		Test Current	Max. Clamping Voltage @ IPP	Max. Peak Pulse Current	Max. Reverse Leakage @ VRWM	Marking code
BI-POLAR	VRWM(V)	Min.(V)	Max.(V)	IT(mA)	VC MAX.(V)	IPP(A)	IR(uA)	
LDP5S24CA	24.00	26.70	29.50	1	38.9	129.0	5	LDP5S24CA
LDP5S26CA	26.00	28.90	31.90	1	42.1	119.0	5	LDP5S26CA
LDP5S28CA	28.00	31.10	34.40	1	45.4	110.0	5	LDP5S28CA
LDP5S30CA	30.00	33.30	36.80	1	48.4	103.0	5	LDP5S30CA
LDP5S33CA	33.00	36.70	40.60	1	53.3	93.9	5	LDP5S33CA
LDP5S36CA	36.00	40.00	44.20	1	58.1	86.1	5	LDP5S36CA
LDP5S40CA	40.00	44.40	49.10	1	64.5	77.6	5	LDP5S40CA
LDP5S43CA	43.00	47.80	52.80	1	69.4	72.1	5	LDP5S43CA
LDP5S45CA	45.00	50.00	55.30	1	72.7	68.8	5	LDP5S45CA
LDP5S48CA	48.00	53.30	58.90	1	77.4	64.7	5	LDP5S48CA
LDP5S51CA	51.00	56.70	62.70	1	82.4	60.7	5	LDP5S51CA
LDP5S54CA	54.00	60.00	66.30	1	87.1	57.5	5	LDP5S54CA
LDP5S58CA	58.00	64.40	71.20	1	93.6	53.5	5	LDP5S58CA
LDP5S60CA	60.00	66.70	73.70	1	96.8	51.7	5	LDP5S60CA
LDP5S64CA	64.00	71.10	78.60	1	103.0	48.6	5	LDP5S64CA
LDP5S70CA	70.00	77.80	86.00	1	113.0	44.3	5	LDP5S70CA
LDP5S75CA	75.00	83.30	92.10	1	121.0	41.4	5	LDP5S75CA
LDP5S78CA	78.00	86.70	95.80	1	126.0	39.7	5	LDP5S78CA
LDP5S80CA	80.00	89.40	98.80	1	130.0	38.5	5	LDP5S80CA
LDP5S85CA	85.00	94.40	104.00	1	137.0	36.5	5	LDP5S85CA

Notes:
(1) Pulse Test: tp≤50ms.
(2) Surge current waveform per Fig. 3 and derated per Fig.2.

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Ratings and Characteristics Curves (Ta = 25℃ unless otherwise noted)

Fig. 1 - Power Derating Curve

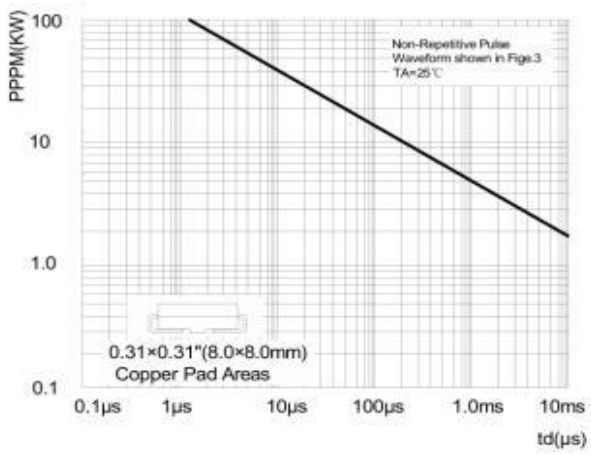


Fig. 2 - Pulse Power or Current vs. Initial Junction Temperature

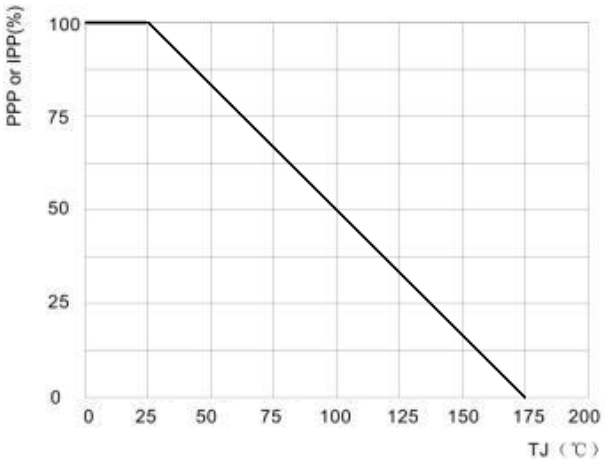


Fig. 3 - Pulse Waveform

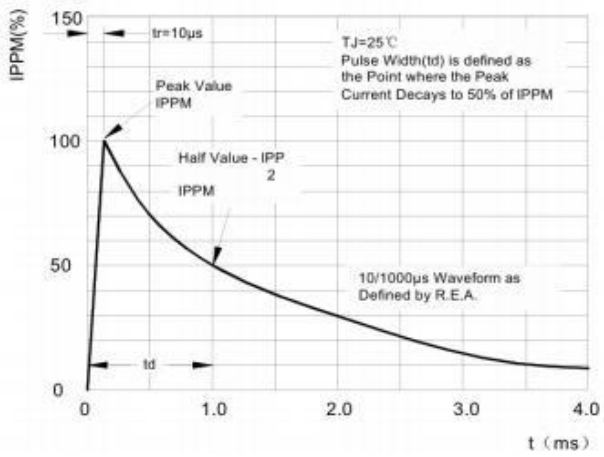


Fig. 4 - Typical Transient Thermal Impedance

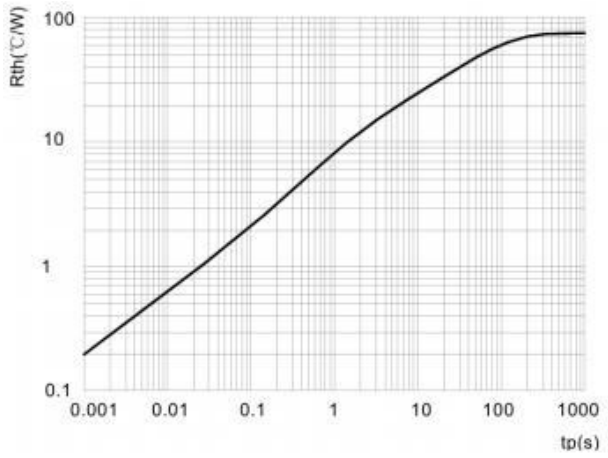


Fig. 5 - Maximum Non-Repetitive Surge Current

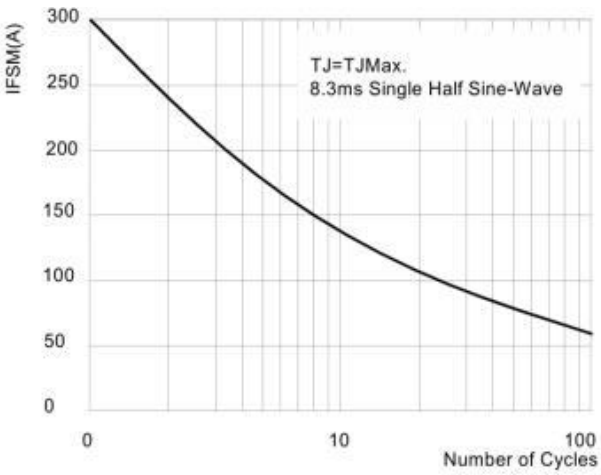
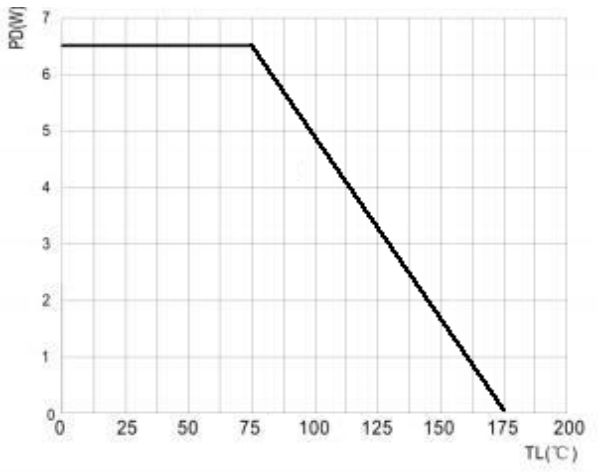


Fig. 6 - Steady State Power Dissipation



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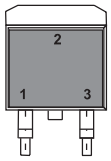
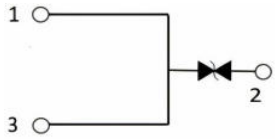
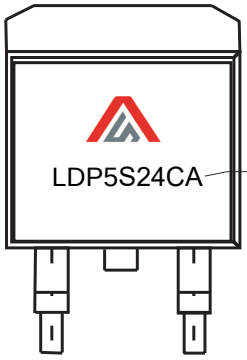
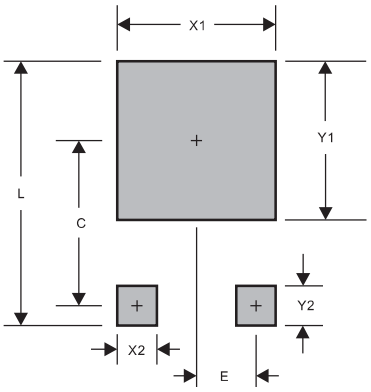
Pinning information

Pin	Simplified outline	Symbol
Pin1 anode Pin2 cathode Pin3 anode		

Marking

Type number	Example
Bi-Directional	

Suggested solder pad layout



PACKAGE	D2PAK
C	0.374(9.50)
E	0.098(2.50)
L	0.665(16.90)
X1	0.425(10.80)
X2	0.071(1.80)
Y1	0.449(11.40)
Y2	0.138(3.50)

Dimensions in inches and (millimeters)